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D E C I S I O N
of 27 January 1994

Case Number: T 0683/91 - 3.5.1

Application Number: 87905897.2 (PCT/US87/02203)

Publication Number: WO 88/02173

IPC: G11C 17/00

Language of the proceedings: EN

Title of invention:
Non-volatile memory cell

Applicant:
NCR Corporation

Opponent:
-

Headword:
-

Relevant legal norms:
EPC Art. 56, 84

Keyword:
"Inventive step (yes) after amendment"

Decisions cited:
.

Catchword:
-

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Case Number: T 0683/91 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 27 January 1994

Appellant: NCR Corporation
World Headquarters
Dayton, Ohio 45479 (US)

Representative: Robinson, R.G.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 22 April 1991 refusing European patent application No. 87905897.2 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: P.K.J. van den Berg
Members: A.S. Clelland
E.M.C. Holtz

Summary of Facts and Submissions

I. European patent application no. 87 905 897.2, based on international application PCT/US87/02203 and published as WO88/02173, was refused by a decision of the Examining Division dated 22 April 1991 on the ground that the subject-matter of independent Claim 1 lacked an inventive step having regard to the following prior art documents:

D1: WO-A-85/03798

D2: 1978 IEEE International Solid-State Circuits Conference, Digest of technical papers, pages 108-109, February 1978.

II. On 17 June 1991 the Applicant lodged an appeal against this decision and paid the prescribed appeal fee. He requested that the decision be cancelled in its entirety and that a patent be granted. On 12 August 1991 a statement setting out the grounds of appeal was received.

III. In a communication pursuant to Article 110(2) EPC dated 9 March 1993 the Rapporteur expressed doubts as to whether Claim 1 was clear and whether its subject-matter involved an inventive step having regard to the disclosure of D1.

IV. In a response received on 17 July 1993 the Appellant argued in support of his claims and as an auxiliary request filed a further set of claims, to be considered if the Board did not accept the claims of the main request.

V. The Appellant's **main** request is the grant of a patent on the basis of the following documents:

Claims: 1 to 7 as originally filed, with the amendment to line 2 of Claim 1 requested in the letter received on 6 February 1991,

Description: pages 1 to 12 as originally filed, with the amendments to page 2, line 7 and page 3, line 13 requested in the letter received on 6 February 1991,
pages 1a and 1b as filed on 6 February 1991,

Drawings: as originally filed.

VI. The Appellant's **auxiliary** request is the grant of a patent on the basis of Claims 1 to 5 as received on 17 July 1993.

VII. Claim 1 according to the **main request** reads:

"A nonvolatile memory cell formed in a semiconductor substrate, comprising: a first conductive path (18) in said semiconductor substrate, between a first bit line (16) and a common control electrode (21), including therein a serial connection of a first access transistor (3) operatively connected to a word line (2), and a first floating gate sense transistor (8); a second conductive path (19) in said semiconductor substrate, between a second bit line (17) and said common control electrode (21), including therein a serial connection of a second access transistor (7) operatively connected to said word line (2) and a second floating gate sense transistor (9); first and second electrodes (13, 14) respectively connected to first and second program lines

(22, 23); a first floating gate electrode (11) adapted to control said first floating gate sense transistor (8), having a first relatively small capacitive coupling to said first electrode (13) and a second relatively large capacitive coupling to said second electrode (14); and a second floating gate electrode (12) adapted to control said second floating gate sense transistor (9), having a first relatively small capacitive coupling to said second electrode (14) and a second relatively large capacitive coupling to said first electrode (13)."

VIII. Claim 1 according to the **auxiliary request** reads:

"A nonvolatile memory cell formed in a semiconductor substrate, comprising a first conductive path (18) in said semiconductor substrate, between a first bit line (16) formed in said semiconductor substrate and a common control electrode (21) formed in said semiconductor substrate, said first conductive path (18) including a first access transistor (3) controlled by a word line (2) formed by a conductive line overlying said semiconductor substrate, and a first floating gate sense transistor (8); a second conductive path (19) in said semiconductor substrate, between a second bit line (17) formed in said semiconductor substrate and said common control electrode (21), said second conductive path (19) including a second access transistor (7) controlled by said word line (2), and a second floating gate sense transistor (9); first and second program line electrodes (13, 14) formed in said semiconductor substrate and respectively connected by third and fourth access transistors (4, 6) controlled by said word line (2) to first and second program lines (22, 23) formed in said semiconductor substrate; a first floating gate electrode (11) overlying said semiconductor substrate and adapted to control said first floating gate sense transistor (8) and having a first, relatively small capacitive coupling

to said first program line electrode (13) and a second, relatively large capacitive coupling to said second program line electrode (14); and a second floating gate electrode (12) overlying said semiconductor substrate and adapted to control said second floating gate sense transistor (9) and having a first, relatively small capacitive coupling to said second program line electrode (14) and a second, relatively large capacitive coupling to said first program line electrode (13)."

IX. The Appellant's arguments in support of the patentability of the subject-matter of Claim 1 of the main request can be summarised as follows.

The claimed invention relates to a non-volatile memory cell having floating gate sense transistors with respective floating gate electrodes; further electrodes, connected to respective program lines, each have a relatively small capacitive coupling to one floating gate electrode and a relatively large capacitive coupling to the other floating gate electrode. A simple structure with only a single polycrystalline silicon layer is possible, whilst a high-speed read-out is enabled.

The arrangement known from D1 also provides a non-volatile memory cell using floating gate transistors but requires the presence of a separate control gate for each transistor in addition to the floating gate. The D1 device moreover does not provide first and second electrodes (providing capacitive coupling) but has programming nodes which the Examining Division has incorrectly identified with the electrodes. Moreover, the Examining Division's contention that the skilled man would without the exercise of invention replace the gate electrode capacitors known from D1 by diffused electrode capacitors is based on an *ex post facto* analysis.

The D1 arrangement is explicitly stated to be suitable for use in storing the location of defects in an EEPROM and is a latch circuit which would not be suitable for use as a cell in a memory array. Claim 1 requires first and second bit lines, which are not identifiable with the DATA OUT lines of D1; these DATA OUT lines give outputs in response to switching of latch transistors and are therefore comparatively slow because of the inherent gate capacitance of these transistors. D1 furthermore does not disclose the use of a "common control electrode" (in the language of Claim 1 of the application) for the floating gate sense transistors, the source of each transistor being in D1 separately connected to the fixed potential V_{ss}.

Nor would the skilled man combine the disclosure of D2 with that of D1 in order to arrive at the claimed invention, D2 merely disclosing the coupling of a floating gate to the drain electrode of the same transistor.

X. As regards the auxiliary request, the Appellant argues that Claim 1 of that request - in addition to the features noted above as distinguishing from D1 - is directed to the structural features of a physical layout which is substantially simpler than that known from D1.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. Claim 1 of the main request is in substance the originally filed claim. Claim 1 of the auxiliary request contains all the features of Claim 1 as originally filed and does not therefore contravene Article 123(2) EPC.

3. *Clarity of Claim 1*

3.1 Claim 1 of the main request gives rise to some doubt as to its interpretation since expressions are used which can be read either as defining a physical layout or as generalised circuit components. In particular, the term "electrode" as used in "common control electrode", and "first and second electrodes" is difficult to reconcile with the constructional features specified in the claim. The expression could, for example, be synonymous with "conductive path" as used in the claim, or it could refer to an ohmic path in a doped semiconductor substrate, or in the extreme case to a piece of wire forming a connection.

The Board notes from Figure 2 of the application that the "conductive paths" 18 and 19, referred to in the description in the paragraph bridging pages 4 and 5 as "n^+ diffusions ... in the p^- doped silicon substrate", are shown in the same hatched lines as the region 21 which is referred to as an "electrode". The Board accordingly concludes that the term "electrode" is to be interpreted as any conductive path and indeed includes a node joining conductive paths.

3.2 A similar interpretation has been adopted as regards the use of the expression "common control electrode" in Claim 1 of the auxiliary request.

4. *Inventive step (main request)*

4.1 D1 discloses in connection with Figures 1a and 2 a non-volatile memory cell 10, formed in a semiconductor substrate 205, comprising a first conductive path D in said semiconductor substrate between a first data out line (at node 28) and a common control electrode V_{ss}; a first floating gate sense transistor 50; a second conductive path in the semiconductor substrate between a second data out line (at node 38) and a common control electrode V_{ss}; a second floating gate sense transistor 70; first and second electrodes 78, 58 respectively connected to first and second program lines (programmer 100); a first floating gate electrode 52 adapted to control said first floating gate sense transistor 50 having a first relatively small capacitive coupling c_t to said first electrode 78 and a second relatively large capacitive coupling c_1 to said second electrode 58; and a second floating gate electrode 72 adapted to control said second floating gate sense transistor 70 having a first relatively small capacitive coupling c_t to said second electrode 58 and a second relatively large capacitive coupling c_1 to said first electrode 78.

4.2 It will be noted that in the above analysis the Board has taken the term "electrode" to mean "conductive path" as indicated at paragraph 3 above, so that the connection from control gates 54, 74 to respective capacitors 76, 57 by way of nodes 78, 58 constitute respective "electrodes" in the sense used in the claim.

4.3 It is observed that for charge transfer to take place in the capacitors 57 and 76 of D1 it is necessary for the

floating gates 52, 72 to be taken to opposing voltage levels; in other words, if one plate of capacitor 57 is at the level of node 78 then the other plate must approximate the level of node 58 by means of capacitive coupling between gates 52 and 54 and between gate 52 and the drain or source of transistor 50. This implies a high capacitance between gates 52 and 54 and a low capacitance for capacitor 57. From Figure 2 of D1 in conjunction with the description at page 8, lines 16 to 31 it can be seen that the capacitor c_t between floating gate 230 and highly doped region B is comparatively small, whilst the capacitor c_1 between floating gate 230 and control gate 240 is comparatively large. From page 9, line 26 to page 10, line 8 of D1 it can be seen that the voltage across capacitor c_t is proportional to a coupling coefficient K where K is equivalent to the value c_1/c_1+c_2 where c_2 is the capacitor between the floating gate and the transistor substrate, i.e. between gate 230 and substrate 205 in Figure 2. The coefficient K is said at page 10, lines 5 to 8 of D1 to have a typical value of 0.8, implying a value for c_1 four times that of c_2. As noted above, c_1 must be many times greater than c_t in order for the programming voltage to be developed across c_t.

4.4 D1 does not disclose the provision of first and second line access transistors in series with respective floating gate sense transistors and operatively connected to a word line.

The subject-matter of Claim 1 is accordingly novel having regard to the disclosure of D1.

4.5 The only difference of substance between the disclosure of D1 and the claimed subject-matter lies in the use of line access transistors. These transistors enable the memory cell to be used as part of a memory array, the

word line serving as row select line and the access transistors for column select. The device known from D1 is referred to at page 13, line 11, as a memory cell and is stated in the introduction to the description to provide a non-volatile memory device which assumes the proper state when power is applied to a circuit and which requires a minimal amount of support circuitry such as sense amplifiers. The prior art from which the device goes out is concerned with memory cells for use in an array, so that the skilled man would understand that the D1 memory device could also be used in an array. The Board accepts that the described embodiment is not in fact such a memory cell but is apparently a stand-alone flip-flop for use in error circuitry in an EEPROM, other stand-alone applications also being discussed at page 13, lines 10 to 17. Nevertheless, the context in which the device is described, in particular the reference at page 13, lines 6 to 9 to construction of the device using the same technology as other elements of the EEPROM of which it forms a part, would lead the skilled man in the direction of using the device as a memory cell of an array. For the skilled man to use the device in such an application it would be necessary to provide bit and word lines for row and column selection. It has been noted by the Board that all the documents cited in the European search report, with the exception of D1, disclose the provision of series transistors for providing such address selection. The Board accordingly considers that the skilled man would not be prejudiced against applying the D1 cell to a memory array; if he were to do so he would without the exercise of invention provide for cell addressing by means of transistors in series with the respective floating gate sense transistors, the usual arrangement in the art. Such an arrangement would fall within Claim 1 of the main request.

4.6 The subject-matter of Claim 1 of the main request accordingly lacks an inventive step.

5. In the Statement of Grounds of Appeal the Appellant has advanced various arguments as to why the skilled man, given the contents of D1, would not arrive at the claimed arrangement. These arguments can be summarised as follows:

(a) the claimed arrangement does not require a separate control gate in addition to the floating gate, as is necessary in D1, only a single polycrystalline layer is therefore necessary;

(b) it is improper to equate the "first and second electrodes" with the "programming nodes" known from D1, since a programming node cannot have a capacitive coupling;

(c) D1 provides a gate electrode capacitor whereas the claimed arrangement uses a diffused electrode capacitor;

(d) D1 does not disclose the provision of a memory cell suitable for use in an array, a latch for use in storing the location of defects in an EEPROM being described;

(e) the DATA OUT lines in D1 are not bit lines;

(f) the inherent gate capacitance of transistors 20, 30 in D1 will result in a slow read rate as compared to the differential read operation of the invention; and

(g) the electrode (21) of the invention is a common **control** electrode; different potentials are applied

to it in dependence on whether a read or write operation is being undertaken, whereas in D1 the V_{ss} line has an unchanging low potential applied to it.

5.2 Dealing with these arguments in turn, Claim 1 is silent as to the presence or absence of a control gate and one or more polycrystalline layers, point (a). This is not therefore a distinguishing feature of the claimed invention. As was pointed out in paragraph 3 above, the expression "electrode" is so broad as to encompass any conductive path, including the conductive paths embracing the programming nodes in D1; point (b) does not therefore provide a distinguishing feature. The distinction being made in point (c) appears to rely on a particular physical layout which is not in fact claimed in Claim 1 of the main request; whether or not the gate electrode capacitor of D1 is a diffused electrode capacitor is accordingly of no consequence, since it does not constitute a claimed feature. Points (d) and (e) are dealt with at paragraph 4.5 above. Point (f) again does not relate to the claimed subject-matter since speed of operation is not explicitly mentioned in the claim; if this point were considered as a technical prejudice which would prevent the skilled man from making use of the D1 arrangement in a memory array, it is observed that if the skilled man were to provide series transistors for bit lines he would appreciate that the transistors 20 and 30 in D1 would no longer be necessary, so that even if speed of operation were an explicit feature of the claim the manner in which the skilled man would modify the D1 circuit for use in a cell array would result in an equally fast cell. Finally, point (g) again relates to a feature which is not claimed since no particular voltages are specified for the common control electrode and in any case voltage measurement is always relative; whether the common control electrode potential is varied and other

potentials are held fixed, or the common control electrode potential is held fixed and the other potentials varied, the result is ultimately the same.

6. *Inventive step (auxiliary request)*

6.1 Claim 1 of the auxiliary request differs from that of the main request in two respects: firstly, the claim specifies a particular physical layout in that various components are said to be formed in or overlying the semiconductor substrate in which the claimed non-volatile memory cell is formed, whilst secondly the subject-matter of appendant Claims 2 and 3 of the main request has been included.

6.2 D1 does not clearly describe a physical cell layout; Figure 2 of D1 serves merely to show the construction of the floating and control gates, and the various capacitive couplings of these gates. The Board considers that the skilled man, starting out from the disclosure of D1 and wishing to construct a non-volatile memory cell for use in an array, would not derive the claimed layout from this document. Moreover, the claim is now restricted to programming by means of third and fourth access transistors controlled by the word line and which connect respective program line electrodes formed in the semiconductor substrate to program lines. In D1 programming is by means of a programming circuit comprising NOR gates and an inverter, the output of the gates being connected to the floating gate sense transistor control gates. This represents an alternative programming arrangement and the skilled man, given the disclosure of D1, would have no reason to modify the disclosed programming arrangement in such a manner as to arrive at that claimed.

6.3 The Board have also considered whether the skilled man, given the disclosure of D1, would be led by another prior art document, cited either in the international search report or in the introduction to the description, both to modify the D1 arrangement so as to arrive at the claimed configuration and to implement the claimed physical construction. The Board do not consider that this is the case; even if, for the sake of argument, the skilled man implementing the D1 arrangement would arrive at a physical layout similar to that of the claim, the remaining prior art would not lead him to modify the D1 programming arrangement so as to arrive at the claimed configuration.

6.4 The Board accordingly concludes that Claim 1 of the auxiliary request is both novel and inventive.

7. Although Claim 1 of the auxiliary request has been held allowable, the Appellant has not yet filed an amended introduction to the description corresponding to the claim. For this reason it is necessary to remit the application to the Examining Division for examination to be completed.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order that further prosecution is to be based on Claim 1 of the auxiliary request filed 17 July 1993.

The Registrar: The Chairman:

M. Kiehl P.K.J. van den Berg