BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Publication in the Official Journal [redacted] / No

File Number: T 943/91 - 3.5.1

Application No.: 87 201 714.0

Publication No.: 0 259 932

Title of invention: Electronic circuit having complementary signal-carrying data lines

Classification: H03M 1/36

D E C I S I O N
of 31 July 1992

Applicant: N.V. Philips' Gloeilampenfabrieken

Headword:

EPC Article 56

Keyword: "Inventive step (yes)"

Headnote

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 943/91 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 31 July 1992

Appellant : N.V. Philips' Gloeilampenfabrieken
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Decision under appeal : Decision of Examining Division of the European Patent Office dated 14 June 1991 refusing European patent application No. 87 201 714.0 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : R. Randes
W.M. Schar

Summary of Facts and Submissions

I. European patent application No. 87 201 714.0, filed on 10 September 1987 and published on 16 March 1988 under No. 259 932, was refused by a decision of Examining Division 068 dated 14 June 1991.

II. The reason given for the refusal was that the subject-matter of Claim 1, filed on 12 September 1990, lacked an inventive step having regard to the prior art in respect of the following documents:

D1: Interface, bipolar LSI, bipolar memory, programmable logic Databook, National Semiconductor corporation, 1983, pages 1-123, "integrated circuits for digital data transmission"

D2: GB-A-2 029 053

D3: GB-A-1 547 918

D4: US-A-4 218 675

The Examining Division found that the skilled man would have arrived at the claimed subject-matter either by combining D3 and D1 or D3, D2 and D4.

III. On 30 July 1991 the Appellant filed a Notice of Appeal against that decision. The appeal fee was paid on 2 August 1991. The Statement of Grounds was filed on 16 October 1991, wherein the Appellant contested the Examining Division's view. The main objection was that both key documents - D1 and D2 - did not relate to the same technical field as the present invention and therefore also solved quite different problems. The skilled person would therefore not have considered these documents.

IV. In response to a communication of the Board pursuant to Article 110(2) EPC, raising objections under Article 123(2) EPC, the Appellant filed on 5 May 1992 a replacement Claim 1 and a replacement page 1 of description. Claim 2 as filed on 12 September 1990 and description pages 2 to 4 as originally filed were left unamended, as well as the originally filed drawing sheet 1/1.

Claim 1 is now worded as follows:

"An electronic circuit arrangement in which selection means select a transistor from a group of (2^n-1) multi-emitter transistors each having n emitters under the control of an input signal and make it conductive, of which emitters a selection is connected to n data lines, which data lines further are each connected on the one hand to a current source and on the other hand to an output circuit for generating at the output of the output circuitry a binary output signal belonging to a given input signal, characterized in that n pairs of data lines are provided, a first and a second data line within a pair belonging to a first and a second group of n data lines, respectively, the i^{th} emitter of each transistor being connected either to the i^{th} data line of the first group or to the i^{th} data line of the second group, the i^{th} data lines forming one of the n pairs of data lines with $1 \leq i \leq n$, so that each pair of data lines always carries complementary logic signals."

V. The Appellant requests that the decision under appeal be set aside and a patent granted on the basis of the documents cited under item IV above.

Reasons for the Decision

1. The appeal is admissible.

2. The subject-matter of present Claim 1 corresponds to the subject-matter of original Claims 1 and 2. However, the number of multi-emitter transistors within a group of multi-emitter transistors has been changed from 2^n as claimed in original Claim 1 to $2^n - 1$. This amendment is clearly allowable and moreover necessary as the original figures and the text of the original description disclose that only the number $2^n - 1$ is used. Therefore the current version of the claims complies with Article 123(2) EPC.

3. The closest prior art to the invention is D3. This document discloses a circuit arrangement corresponding to the prior art portion of Claim 1. The subject-matter of Claim 1 is novel, as its characterising features are not disclosed by D3.

4. It is therefore left to be decided, whether the subject-matter of Claim 1 involves an inventive step.

4.1 In such known circuit arrangements (cf. the simplified circuit of Figure 1 in the present application and page 1, second paragraph of the description) the data on the data lines are compared with a reference voltage by an output circuit to establish whether the data lines carry a logic high or logic low signal. Therefore the circuit has a low interference margin and usually it is not possible to increase the difference between the logic low and high signal, because only a small voltage range is available.

The objective problem to be solved, therefore appears to be to provide an electronic circuit arrangement in which the interference sensitivity is reduced.

4.2 D1 relates to data transmission between an independent transmission unit and a remote independent receiver unit, which are connected by a twisted-pair line as shown in Figure 1b in order to compensate induced voltages introduced on the transmission line. This is an improvement in relation to the arrangement shown in Figure 1a, wherein ground is used as a signal return and wherein the voltage seen at the receiving end is the output voltage of the transmitter plus any noise voltage induced on the line. Thus this document appears to indicate in which way a transmission between two units can be improved and appears in no way to indicate how said objective problem could be solved, i.e. to generate insensitive signals in an arrangement according to the preamble of valid Claim 1.

As has been noted by the Appellant (Grounds of Appeal) having regard to the prior art (Figure 1 of the application), there are no signals available to provide complementary signals and the prior art does not suggest that unused emitters of multi-emitter transistors could be used to this effect (D1 shows no transistors at all). Moreover, according to the invention the used "unused emitters" do not provide the complementary signals, they merely provide exactly the same signals as the used emitters, but on different extra data lines.

4.3 D2 teaches how it is possible to recognise in programmed store matrices stored information which has been subsequently altered, and to exclude the altered information from retransmission. The example disclosed in D2 discloses a store matrix 1 with word addresses 13 of four bits each. In contrast to conventional arrangements, the coupling points and the read out wires are duplicated, i.e. each read out "line" is made up of a pair of wires (A

and A', B and B' etc.). Programming is effected in the manner that in each case two coupling points associated with a data bit of the same word address assume opposite states after programming, which can be read out in conventional manner over the readout wires A to D and, in the inverted manner over the readout wires A' to D'. Each pair of read out wires (e.g. A and A') is connected to an input of an exclusive-OR gate (2 to 5). As far as the information read is true (complementary signals on a pair of wires), the output of the exclusive-OR gate is at H-level. However, if the store content has been altered after completed programming, the output of the gate concerned will be at a L-level. The outputs from the exclusive-OR gates are used to block a switch connected to the readout wires A to D (leading the uninverted signals to the output of the arrangement) when a store content has been changed after programming.

Thus D2 does not teach how the sensitivity of a signal can be decreased. It just happens that it shows that a signal and accidentally its complementary signal is used to detect whether a programmed store content has been erroneously altered or not. As the Appellant has observed (Grounds of Appeal), the method according to D2 "would work just as well if the words were stored twice in their non-complementary form in the pair of locations and EXOR-gates would be replaced by AND-gates". The complementary signals in D2 are only used as redundant information to detect an error in the original information. According to the invention, however, the complementary signals are used to provide to the output circuit a larger voltage difference. A connection cannot therefore be detected between the said objective problem to be solved and the teaching of D2.

Moreover, the Board does not agree with the identification made in the impugned decision of the features of the arrangement according to Figure 3 of D2 and which correspond to the ones of Claim 1.

The control circuit 2 to 7 cannot be considered as part of the output circuit, because such output circuit in correspondence to the present application should be connected to the terminals A,B,C and D (at right hand side of Figure 3 in D2). Thus the teaching of D2 does not, as the arrangement according to Claim 1, disclose pairs of data lines connected to the real output circuit, since only one data line in a pair (the one having the uninverted signal) in said arrangement in D2 is connected to this output circuit, pairs of data lines are instead connected to the input of the control circuit (2 to 6), the output of which controls the said switch 7.

Moreover, the interpretation of the arrangement according to Figure 3 of D2 given in the impugned decision is based on the case that the matrix is appropriately programmed. Apparently only those diodes of the matrix which are not disconnected (n diodes in each column - cf. reference sign 12, Figure 2) have been considered. It appears to the Board that it would be more appropriate to consider the whole programmable matrix structure, which, however, apparently has 2^n diodes in each column. It therefore does not appear to be obvious that the skilled man would replace the diodes in each column by a multi-emitter transistor having n emitters as suggested in the impugned decision. The reference to D4 was apparently made there only in order to demonstrate that multi-emitter transistors can be used in similar circuits (ROM input section).

4.4 The Appellant has realised that the interference sensitivity of the known electronic arrangement (Figure 1 of the application) can be reduced by using the normally unused emitters of the transistors and by connecting them to the other group of data lines introduced by the Appellant. This new arrangement works more reliable than the old one, does not need a separate reference voltage and, moreover, does not need more space than the prior art chip, which also the Examining Division has implicitly recognised (decision, under 12b, page 5, first paragraph "since such a design would minimise the required chip space").

5. For the foregoing reasons, the Board has come to the conclusion that the subject-matter of Claim 1 would not be obvious from the prior art relied on by the Examining Division.

6. It follows that Claim 1 is acceptable under Article 52(1) EPC.

The same applies to the dependent Claim 2.

7. In the documents indicated in paragraph IV above, the following clerical errors should be rectified:

- Description, page 3, line 21, "$\overline{D1}$" should read "D1"
- Description, page 3, line 27, "D" should read "D1"
- Figure 1, at data line D3, the third (from the left hand side) logic symbol "1" should read "0".

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the Appellant's request according to paragraph V above, with correction of the clerical errors noted in paragraph 7 above.

The Registrar: The Chairman:

M. Kiehl P.K.J. van den Berg

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