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D E C I S I O N
of 5 September 1995

Case Number: T 0085/92 - 3.4.1

Application Number: 84200308.9

Publication Number: 0118158

IPC: H01L 29/68

Language of the proceedings: EN

Title of invention:
Programmable read-only memory structure and method of fabricating such structure

Applicant:
Philips Electronics N.V.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 84
EPC R. 29, 27

Keyword:
"Clear and supported by the description (after amendment, yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0085/92 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 5 September 1995

Appellant: Philips Electronics N.V.
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Representative: Veerman, Jan Willem
INTERNATIONAAL OCTROOIBUREAU B.V.,
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 10 September 1991 refusing European patent application No. 84 200 308.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. D. Paterson
Members: H. J. Reich
U. G. O. Himmler

Summary of Facts and Submissions

I. European patent application No. 84 200 308.9 (publication No. 0 118 158) was refused by a decision of the Examining Division.

II. The reason given for the refusal was that independent method Claim 15 as filed on 20 March 1991 violates Article 84 EPC, because the claimed sequence of processing steps (c) and (d) - first (c), i.e. the implantation for converting the second or surface region of the first region to amorphous form and thereafter (d), i.e. the doping to form a low resistance contact region - is the opposite to that in all the embodiments disclosed and is thus **not supported** by the description. According to the description the contact region as formed in step (d), is produced by diffusion or by implantation and annealing. Such heat treatment in step (d) when performed **after** conversion step (c) would anneal the region which had previously been made amorphous. No disclosure of the reversed operation can be found in the description. Independent Claim 1 filed 20 March 1991 was considered as satisfying all requirements of the EPC.

III. The Appellant lodged an appeal against this decision and requested grant on the basis of the claims filed on 20 March 1991 as his main request; on a Claim 15 wherein step (d) had been deleted, as his first auxiliary request; and on a Claim 15 wherein steps (c) and (d) had been interchanged as his second auxiliary request. Furthermore he requested auxiliary oral proceedings.

IV. In a communication pursuant to Article 110(2) EPC the Board informed the Appellant of its provisional view that Claim 15 of his main request was considered to be in contradiction to the embodiments disclosed and thus not allowable under Article 84 EPC; that Claim 15 of the first auxiliary request appeared to be allowable after the introduction of some minor amendments; and that inter alia independent Claims 1 and 15 did not satisfy Rule 29(1)(a) EPC having regard to documents:

D1: IBM Technical Disclosure Bulletin, vol. 24, No. 7A, December 1981, pages 3460 to 3461, and

D2: GB-A-2 065 972.

Document D1 was considered to be the prior art closest to Claim 15 and document D2 the prior art closest to Claim 1. Corresponding amendments of claims and description were proposed.

V. In reply to the Board's communication the Appellant filed on 14 July 1994 a new set of claims with adapted description pages as his main request. The Board regarded this new set of claims and the adaptation of the description as still not satisfying Rules 29 and 27 EPC. Following a consultation between the Rapporteur and the Appellant by telephone on 8 June 1995, a letter of the Appellant dated 17 July 1995 and a further consultation between the Rapporteur and the Appellant by telephone dated 11 August 1995, the Appellant now requests that a patent be granted on the basis of the following main request:

Claims: 1 to 16 filed 18 July 1995 with letter dated 17 July 1995 and with the amendment in Claim 1 requested 11 August 1995.

Description: Pages 1, 2, 2a filed 18 July 1995 with letter dated 17 July 1995 and with the amendments on pages 2 and 2a requested 11 August 1995;
Pages 3 to 10 according to EP-A-0 118 158.

Drawings: Sheet 1/4 to 4/4 according to EP-A-0 118 158.

VI. The independent claims of the main request read as follows:

"1. A semiconductor memory structure, comprising: a semiconductor body having a surface layer of first type conductivity; a first region adjoining the surface and producing a rectifying junction with a selected portion of said surface layer; a second region formed on top of said first region; a buried layer of first type conductivity extending into said surface layer and beneath said second region, said buried layer being heavily doped to form a low resistance path; said surface layer, said first region and said buried layer being crystalline in form, said second region being amorphous in form, characterized in that the first region is formed by a region of the second type conductivity provided in the surface layer, said rectifying junction being formed by the pn-junction between the first region and the surface layer, the second region being formed in the first region and extending to the surface of said surface layer, and in that a third region of first type conductivity is formed in a selected portion of said surface layer laterally spaced from said first and second regions, said third region being heavily doped to have a higher conductivity

than said surface layer, the buried layer of first type conductivity extending beneath both said third region and said first and second regions.

8. A method of fabricating a semiconductive programmable read only memory structure comprising implanting ions of sufficiently high energy and density within a surface layer of a body portion of crystalline semiconductor material of first type conductivity to convert said surface layer locally to amorphous form that is electrically and irreversibly switchable from high resistance state to low resistance state, characterized by the following sequence of steps:

(a) locally oxidizing selected surface regions of a body portion of crystalline semiconductor material of first type conductivity to produce a plurality of laterally isolated semiconductor regions in said body portion;

(b) introducing dopant impurities of second type conductivity in a first one of said isolated semiconductor regions to produce a first region of second type conductivity forming a semiconductive junction with said body portion at a location beneath the surface of said body portion;

(c) implanting ions of sufficiently high energy and density within a surface layer of said first region to convert said surface layer to amorphous form and that is electrically and irreversibly switchable from high resistance state to low resistance state."

Claims 2 to 7 are dependent on Claim 1 and Claims 9 to 16 are dependent on Claim 8.

VII. In support of this main request the Appellant argued essentially as follows:

(a) The invention relates to a semiconductor memory structure in which a rectifying junction and a programmable element (formed by said second or surface region of the first region which comprises amorphous semiconductor material and is irreversibly switchable from a high-resistance state to a low-resistive state) are vertically integrated within the semiconductor body in order to save valuable chip area.

(b) Claim 8 describes in steps (a) through (c) a method of manufacturing such a memory structure and how the vertical integration may be achieved. Step (d) merely gives a possibility of contacting the body portion of the rectifying junction at the surface, is thus not essential to the invention and can accordingly be omitted from Claim 8.

(c) Though not mentioned in the description, carrying out step (d) after step (c) leads to a usable structure and is by no means speculative. A skilled person is familiar with doping treatments which do not require a heat treatment that would recrystallise the amorphous surface layer. Such "rapid thermal anneal" may be carried out to activate introduced impurities without deteriorating the amorphous region of the antifuse.

Reasons for the Decision

1. The subject-matter of Claims 1 to 7 of the main request corresponds to that of original Claims 1 to 7; the subject-matter of Claim 8 corresponds to the technical features defined in steps (a), (b) and (c) of original Claim 15; the subject-matter of Claim 9 corresponds to the technical features defined in step (d) of original Claim 15; and the subject-matter of Claims 10 to 16 corresponds to that of original Claims 16 to 22. The amendments of the description are in line with Rules 27(1)(b), (c) EPC. There is therefore no objection under Article 123(2) EPC to the current set of application documents.

2. *Claims 8 and 9 - Article 84 EPC*

2.1 The subject-matter of present Claim 8 no longer contains method step (d) as in the wording of corresponding Claim 15 which was filed 20 March 1991 and was rejected by the Examining Division under Article 84 EPC. Thus, an annealing or diffusion step following the production of the amorphous surface layer is no longer comprised in the subject-matter of Claim 8. Claim 8 is therefore supported by the description and no longer speculative. The method of fabrication according to Claim 8 is furthermore technically consistent with the two embodiments of the invention disclosed in Figures 2 to 7 and 11 to 13 respectively. The fact that the formation of N^+ contact region 54 according to Figure 7 has no longer an explicit counterpart in the subject-matter of Claim 8 does not contradict the claim wording because of its open formulation: "A method ... comprising". This

means that any further specification and any supplement of the claimed sequence (a), (b) and (c) by additional method steps is not excluded by the present wording of Claim 8.

2.2 The objective problem underlying the present invention is based on the advantages disclosed in the description, page 10, lines 13 to 25, and consists in manufacturing a semiconductive programmable read-only memory structure with an antifuse by a process which facilitates the use of tighter tolerances and allows smaller circuit sizes. This problem is solved by steps (a), (b) and (c) of Claim 8, wherein the implanted antifuse having reference number 60 in the embodiments, is formed self-aligned according to the wording in step (c): "within a surface layer of the first region" forming a semiconductive junction, i.e. within a region of the semiconductor body or body portion itself. Hence, Claim 8 contains all essential features of the invention.

2.3 The measures of originally disclosed method step (d) produce a contact region to the semiconductor body portion; see also the description page 6, lines 7 to 19. This contact region (see 54 in the embodiments) is spaced apart from the antifuse (60) and serves exclusively as a conductive connection. Hence, original method step (d) has no technical influence on the production of the antifuse and its function, and therefore does not contribute to the solution of the problem underlying the present invention. Method step (d) now forms the subject-matter of Claim 9 which is dependent of Claim 8. The wording of Claim 9 is deliberately chosen not to specify the position of the production of the contact region within the time sequence of steps (a), (b) and (c) claimed in Claim 1. On the one hand, this open formulation allows the disclosed embodiments (with (d) **before** (c)) to fall

within the protection claimed. On the other hand, the Board regards it to be highly likely that the undisclosed rapid thermal anneal - as submitted by the Appellant according to paragraph VII-(c) above - is a well established technique among skilled persons and allows a successful production of a usable cell with step (d) **after** step (c). Therefore, the Board considers that it is justified not to narrow the subject-matter of dependent Claim 9 to a particular position in the time sequence claimed in Claim 1.

2.4 Since independent method Claim 8 automatically results in the antifuse structure comprised in the subject-matter of Claim 1, any explicit reference to Claim 1 is superfluous in order to clarify the subject-matter of Claim 8 or to satisfy Rule 30 EPC; see the appealed decision, page 9, paragraph 3. Moreover, the Board sees no legal reason to limit the method of Claim 8 to the fabrication of a structure having a buried layer (third region) as claimed in Claim 1.

2.5 For the reasons set out in detail in paragraphs 2.1 to 2.4 above, the present wording of Claims 8 and 9 of the main request is considered to satisfy Article 84 EPC.

3. Novelty and inventive step have not been in issue in the present appeal proceedings. The Board agrees with the first instance that it was not obvious in view of the prior art documents cited in the European Search Report, to provide an antifuse - i.e. the surface layer claimed - as a part of the semiconductor body itself; see the communication of the Examining Division dated 5 September 1990, paragraph 1. Hence, independent Claims 1 and 8 (former 15) satisfy Article 52(1) EPC. Dependent Claims 2 to 7 and 9 to 16 concern particular embodiments of the respective independent claim.

Order

For these reasons it is decided that:

1. The decision of the Examining Division is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the following text:

Claims: 1 to 16 filed 18 July 1995 with the amendment in Claim 1 requested 11 August 1995;

Description: Pages 1, 2, 2a filed 18 July 1995 with the amendments on pages 2 and 2a requested 11 August 1995;
Pages 3 to 10 according to EP-A-0 118 158.

Drawings: Sheet 1/4 to 4/4 according to EP-A-0 118 158.

The Registrar: The Chairman:

M. Beer G. D. Paterson