BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS | BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE | CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

A		B		C	X

File Number: T 291/92 - 3.5.2

Application No.: 85 109 701.4

Publication No.: 0 173 108

Title of invention: Electrostatic discharge protection circuit with variable limiting threshold for MOS device

Classification: H02H 9/04

D E C I S I O N
of 27 January 1993

Applicant: KABUSHIKI KAISHA TOSHIBA, et al

Headword:

EPC Articles 56 and 123(2)

Keyword: "Inventive step - yes"
"Added subject-matter - no"

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 291/92 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 27 January 1993

Appellant : KABUSHIKI KAISHA TOSHIBA
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi
Kanagawa-ken 210 (JP)

Representative : Lehn, Werner, Dipl.-Ing.
Hoffmann, Eitle & Partner
Patentanwälte
Arabellastrasse 4
W - 8000 München 81 (DE)

Decision under appeal : Decision of the Examining Division of the European Patent Office dated 28 October 1991 refusing European patent application No. 85 109 701.4 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : R.E. Persson
Members : W.J.L. Wheeler
M.R.J. Villemin

Summary of Facts and Submissions

I. The appeal contests the decision of the Examining Division refusing European patent application No. 85 109 701.4. The reason given for the refusal was that Claim 1 according to the main request infringed Article 123(2) EPC and Claims 1 to 4 according to the auxiliary request did not involve an inventive step. The following prior art documents were cited:

D1: IBM Technical Disclosure Bulletin, Vol. 22, No. 10, March 1980, pages 4452 and 4453: "Voltage programmable protect circuit"

D2: EP-A-0 042 305

D3: GB-A-910 430.

II. In oral proceedings held on 27 January 1993, the Appellant filed an amended description, claims and drawings.

Claim 1 is worded as follows:

"A semiconductor integrated circuit arrangement comprising: an integrated circuit device (13) containing an input MOS transistor (12) responsive to an input signal;

an input terminal (11), coupled to said input MOS transistor (12), for receiving said input signal; and

an electrostatic discharge protection circuit comprising: limiter means (15A) coupled to said input MOS transistor (12) and responsive to a given threshold control potential (Vb), for limiting at a variable threshold the electrostatic potential applied to the gate of said input MOS transistor (12), said threshold being variable according to said given threshold control potential (Vb),

characterized in that said limiter means (15A) includes a bipolar transistor (15A) whose emitter-collector path is inserted between the gate of said input MOS transistor (12) and a fixed reference potential and the base of said bipolar transistor (15A) is connected to receive said given threshold control potential (Vb)."

Claims 2 to 4 are dependent on Claim 1.

III. The Appellant argued essentially that the most relevant prior art document was D1, which disclosed an integrated circuit arrangement in accordance with the prior art part of Claim 1. The limiter means comprised a gated diode (16). There was no evidence to support the Examining Division's assertion that it was obvious to replace the gated diode by a bipolar transistor. In D2 the limiter means comprised a depletion mode MOS transistor (TrP) which conducted when no power was applied to the circuit and was switched off when power was applied. It was not obvious how that circuit could be adapted to incorporate a variable threshold. An indication that it was not obvious to a person skilled in the art to use a bipolar transistor to protect an MOS device could be found in US-A-4 282 556 (D6). There it was recognised that a gated diode occupied an undesirably large area on the chip, but the solution proposed involved only MOS/SOS devices, see column 2, lines 21 to 42. D3 showed a bipolar transistor used as a protection device, but there the base of the transistor was connected via a Zener diode to the input line. Furthermore, D3 dated from 1961, before integrated circuits were known. Pages 182 and 183 of the book "The art of electronics" (D8, submitted in the oral proceedings) showed overvoltage protection circuits (Figures 5.8 and 5.9) comprising a Zener diode and an SCR and a Zener diode and a bipolar transistor. The present

invention used the bipolar transistor in a new way, not requiring a Zener diode, to provide a compact, high conductivity, variable threshold overvoltage protection device comprising only a single component.

IV. The Appellant requested that the decision under appeal be set aside and a patent granted on the basis of the description, claims and drawings filed in the oral proceedings, namely:

Claims 1 to 4, pages 1 to 4, 4a and 5 of description, and one sheet of drawings containing Figures 1 and 2.

Reasons for the Decision

1. The appeal is admissible.

2. In the opinion of the Board, the amendments made comply with Article 123(2) EPC.

2.1 Apart from minor differences in punctuation, the present Claim 1 is the same as Claim 1 according to the main request presented in the oral proceedings held before the Examining Division. In the opinion of the Board, the objections raised against this claim under Article 123(2) EPC (see paragraph 2 of the reasons given in the decision under appeal) cannot be upheld. All the features in the present Claims 1 to 4 can be found in the originally filed application, see for example Claims 1 and 8 to 11 and page 7, lines 8 to 28. The deletion of the phrase "for limiting the potential of an input signal having a given high (e.g., 21V) or low (e.g., 5V) voltage," (which appeared in the original Claim 1) does not contravene Article 123(2) EPC: the "for" phrase is to be interpreted as meaning "suitable for" and the presently claimed

arrangement is clearly not unsuitable for limiting the potential of an input signal having a given high or low voltage; furthermore, it is mentioned at the top of page 8 of the originally filed application that the MOS-input circuit may include a MOS-input analog circuit.

3. Novelty is not in dispute. The closest prior art is D1, which discloses an integrated circuit arrangement in accordance with the prior art part of Claim 1 of the present application. In D1 the protection circuit includes a gated diode connected between the gate of an input MOS transistor to be protected and the circuit ground. The electrostatic potential which may be applied to the gate of the input MOS transistor is limited to a threshold which is variable in dependence on the control potential applied to the gate of the gated diode.

4. As was correctly recognised by the Examining Division, the subject-matter of Claim 1 differs from this prior art in that the limiter means includes a bipolar transistor whose emitter-collector path is inserted between the gate of said input MOS transistor and a fixed reference potential and the base of the bipolar transistor is connected to receive the threshold control potential.

5. The Appellant has pointed out that, given the well known characteristics of bipolar transistors connected in common base mode, it can provide a quicker discharge than a gated diode, while occupying a smaller area on the chip. Although this is not disclosed in the present application, it is, in the opinion of the Board, clear to a person skilled in the art that the present invention offers these advantages.

6. In the opinion of the Board, it is obvious to a person skilled in the art to want to obtain the best possible

electrostatic discharge protection by the use of means occupying the least possible chip area.

7. However, while the Board agrees with the Examining Division that the person skilled in the art can be expected to know the characteristics of bipolar transistors and circuits already existed in which MOS and bipolar transistors were integrated on the same substrate (e.g. MOS to ECL buffer circuits), the Board does not agree that the skilled person would consider the modification of the prior art circuit known from D1 to include a bipolar transistor instead of the gated diode as one of a reduced number of suitable design possibilities.

8. As the Appellant has correctly pointed out, none of the cited prior art documents concerned with protecting MOS integrated circuits from electrostatic discharge mentions using a bipolar transistor for this purpose at all. They all stay within MOS/SOS technology. US-A-4 282 556 (D6) recognises that a gated diode occupies an undesirably large chip area and teaches that chip area may be saved by using a particular arrangement of MOS transistors instead of a gated diode, thus pointing away from the present invention. EP-A-0 042 305 (D2) teaches the use of a depletion mode MOS transistor.

9. Clamp circuits in which excessive voltage is discharged through the emitter-collector path of a bipolar transistor are known per se from GB-A-910 430 (D3) and the book cited by the Appellant (D8), but in these circuits the base and the collector of the transistor are connected to each other via a Zener diode, the base is not connected to receive a given threshold control potential and the threshold is not variable.

10. It therefore appears that the use of a bipolar transistor connected in the way specified in the present Claim 1 was not a readily available workshop alternative to the gated diode. In the opinion of the Board, the subject-matter of Claim 1 involves an inventive step within the meaning of Article 56 EPC. The same applies to the subject-matter of Claims 2 to 4, which are properly dependent on Claim 1.

11. The description has been amended to acknowledge the relevant prior art, namely D1 and D2, and to adapt it to the present Claim 1. Figures 2 to 5 of the original drawings and the related description have been deleted.

12. The Board takes the view that the present application and the invention to which it relates meet the requirements of the EPC.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent in accordance with the Appellant's request (see paragraph IV above).

The Registrar: The Chairman:

M. Kiehl E. Persson

00411