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D E C I S I O N
of 18 October 1995

Case Number: T 0373/92 - 3.4.1

Application Number: 86112483.2

Publication Number: 0216246

IPC: H01L 27/10

Language of the proceedings: EN

Title of invention:
Semiconductor programmable memory device

Applicant:
FUJITSU LIMITED

Opponent:
-

Headword:
Programmable memory device/FUJITSU

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - yes (after amendments)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0373/92 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 18 October 1995

Appellant: FUJITSU LIMITED
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Decision under appeal: Decision of the Examining Division of the European Patent Office dated 25 November 1991 refusing European patent application No. 86 112 483.2 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: G. D. Paterson
Members: R. K. Shukla
U. G. O. Himmler

Summary of Facts and Submissions

I. European patent application No. 86 112 483.2 was refused by a decision of the Examining Division on the ground that the subject matter of the independent claim 1 did not involve an inventive step as required by Articles 52 and 56 EPC in view of the prior art represented by

D1= US-A-4 322 822 and
D2= EP-A-0 089 457.

II. The independent Claim 1 forming the basis for the above decision reads as follows:

"1. A semiconductor programmable device

having a plurality of memory cells (V) each of which is composed of a series connected capacitor (C) and means (D) for blocking current in definite direction,

said memory cells having said capacitor (C) such as the thickness of an insulation layer (34,42,46) of said capacitor (C) is smaller than a definite value so that said capacitor (C) causes break down forming a bypass circuit in said insulation layer when a definite voltage is applied, said definite voltage corresponding to control signal voltage for writing, and

said memory cells are formed on a semiconductor substrate (10) and are isolated from each other, and

each of said capacitors is composed of a plane insulation layer (34,42,46) sandwiched between a plane first semiconductor layer (10) and a plane second semiconductor layer (10a,44), said plane insulation

layer, said plane first semiconductor layer and said plane second semiconductor layer are parallel to each other,

said semiconductor programmable device being characterized in:

said first semiconductor layer (10) and said second semiconductor layer (10a,44) have the same conductivity type and

each of said means (D) for blocking current comprises a device (PN) for passing current in one direction and blocking current in the reverse direction."

III. According to the above decision, document D1 discloses a semiconductor programmable device having a V-shaped dielectric capacitor layer surrounded by semiconductor layers on each side, and in view of document D2 disclosing a planar capacitor structure it would be obvious to modify the device of document D1 such that the layers forming the capacitor are planar instead of V-shaped.

IV. The Applicant lodged an appeal against the decision and filed two sets of claims forming the basis of a main and an auxiliary request, respectively. Claim 1 of the main request was directed to the embodiments described with reference to Figures 8 and 9 as originally filed, and the appellant accordingly also filed revised description and drawings.

The Appellant submitted that amended claim 1 was limited to a semiconductor device in which two semiconductor layers are disposed side by side on a substrate and separated from each other by an insulation layer which extends orthogonally to the surface of the substrate. It

was also submitted that none of the cited documents gave any suggestion which would have lead a skilled person to the claimed device, which facilitated an increase in the integration density of the device and improvement in its speed of operation.

V. In a communication pursuant to Article 110(2) EPC, the Board informed the Appellant that the application as filed was concerned exclusively with a memory device which is programmable by the break down of a capacitor dielectric, and that since the amended claim 1 did not contain any feature to this effect, the application contravened Article 123(2) EPC. Furthermore, the Board informed the Appellant that claim 1 was not clear (Article 84 EPC) in so far as it required that the blocking means blocked the current in a "definite" direction, since in an embodiment of the invention employing a field effect transistor, the flow of current is blocked in either direction so long as the gate is not appropriately biased.

VI. In response to the above communication, the Appellant submitted, with a letter dated 30 March 1995, a new set of claims and an amended page 6 of the description, and requested the grant of a patent on the following documents:

Description: pages 1 to 5 and 7 to 19 filed with the letter of 6 April 1992;
page 6 filed with the letter of 30 March 1995;

Claims: 1 to 9 filed with the letter of 30 March 1995;

Drawings: Sheets 1/4 to 4/4 filed with the letter of 6 April 1992.

In a telephone consultation with the Rapporteur on 18 August 1995, the Appellant agreed to the following amendments to the above mentioned documents:

Description: deletion of reference numerals in lines 5 and 6 on page 6;

deletion on page 14 of the wording, "as vertical type, because the diode and capacitor are arranged vertically in the substrate. But it is possible to provide";

Claims: insertion in claim 5 of "1 to 3" after "preceding claims";

deletion in claim 8 of "or 5" and "from a direction orthogonal to the surface of said substrate (10)"; and

deletion in claim 9 of "4 or" and "from a direction orthogonal to the surface of said substrate (10)".

VII. Independent device claim 1 has the following wording:

"1. A semiconductor programmable device having a plurality of memory cells each of which is composed of a series connected capacitor and a blocking means for blocking current, said memory cells are formed on a substrate (10), each memory cell comprises a first and a second semiconductor layer (44;56,58) and a first insulation layer (46) therebetween, whereby the capacitor of said memory cell is formed, said memory cell being programmable by applying a high voltage to said capacitor and forming a bypass circuit in said

insulation film (46) of said capacitor by dielectric breakdown of said insulation film (46),
characterized in that
said substrate (10) is covered at least partly with a second insulation layer (42) on which said first and second semiconductor layers (44;56,58) and said first insulation layer (46) are formed, and that said first insulation layer (46) is extending orthogonally to the surface of said substrate (10)."

The amended method claims 8 and 9 have the following wording:

"8. A method of fabricating a semiconductor programmable device according to claim 4, characterized in that, said first insulation layer (46) is formed by ion-implanting oxygen atoms into a predetermined region across each of said semiconductor layers (44,56)."

"9. A method of fabricating a semiconductor programmable device according to claim 5, characterized in that said first insulation layer (46) is formed by ion-implanting nitrogen atoms into a predetermined region across each of said semiconductor layers (44,56)."

Reasons for the Decision

1. *Amendments*

Claim 1 is essentially supported by the originally filed claims 1 and 7. Furthermore, as shown and described in the embodiments of Figures 8 and 9 of the application as filed, the memory cells are formed on a substrate (10) and the substrate is at least partly covered by a second insulation layer (42), as stated in the claim. Moreover,

Figures 8 and 9 show that the first insulation layer (46) extends orthogonally to the surface of the substrate. The Board is thus satisfied that the independent claim 1 fulfils the requirement of Article 123(2) EPC. The Board also finds that amendments to claims 2 to 9 do not go beyond the content of the application as filed.

The description and the drawings have been amended to bring them into conformity with the subject-matter of claim 1 by deleting Figures 6 and 7 and the corresponding description, as filed.

The application as amended, therefore, does not contravene the requirement of Article 123(2) EPC.

The only issue which remains to be considered in the present appeal is, therefore, that of inventive step.

2. *Inventive step*

2.1 Claim 1

Document D1 represents the closest prior art and discloses (see in particular Figures 2, 3 and 4), in the wording of the claim under consideration, a semiconductor programmable device having a plurality of memory cells (see column 2, lines 4 to 10) each of which is composed of a series connected capacitor (10) and a blocking means for blocking current (the transistor Q works as a current blocking means), said memory cells are formed on a substrate (21), each memory cell comprises a first and a second semiconductor layer (16 and 17 in Figure 3) and a first insulation layer (22) therebetween, whereby the capacitor of said memory cell is formed, said memory cell being programmable by applying a high voltage to said capacitor (10) and

forming a bypass circuit in said insulation film (22) of said capacitor by dielectric breakdown of said insulation film (see column 2, lines 27 to 35).

In the semiconductor device according to document D1, a semiconductor region (16) located in a semiconductor substrate (21) forms one electrode of the capacitor, a semiconductor layer (17) provided on a capacitor dielectric (22) forms the second electrode of the capacitor and the capacitor dielectric is provided in V-shaped groove formed in the surface of the semiconductor substrate.

In the semiconductor device as claimed in claim 1 of the application in suit, on the other hand, the capacitor is isolated from the substrate by an insulation layer (the "second insulation layer (42)) by providing first and second semiconductor layers forming the capacitor electrodes and a capacitor dielectric layer (the "first insulation layer (46)) on the second insulation layer (42). Moreover, the capacitor dielectric layer (46) extends orthogonally to the substrate surface, so that a lateral arrangement of the capacitor structure is obtained.

Thus, in the semiconductor device of the present invention, the surface of the semiconductor substrate is not utilised for the formation of a capacitor electrode therein, so that more surface area of the substrate is available for the formation of other device elements, which in turn increases the integration density of the device.

In document D2, the semiconductor region (19) forming one of the electrodes (19) of a programme transistor (13) is located in the substrate (see, for example

Figures 3a to 3d; and pages 5 and 6) and an insulation layer (18) which is subjected to a breakdown for programming extends parallel to the substrate surface.

In the Board's view, therefore, the prior art disclosed in documents D1 and D2 do not suggest a lateral capacitor structure isolated from the semiconductor substrate, as claimed in claim 1, so that for a skilled person concerned with improving the integration density of a device such as disclosed in document D1, the subject-matter of claim 1 was not obvious.

For the foregoing reasons, in the Board's judgment, the subject-matter of claim 1 meets the requirement of inventive step within the meaning of Article 56 EPC.

2.2 Claims 2 to 7

These claims are dependent claims and relate to particular embodiments of the invention as defined in claim 1. These claims therefore meet the requirement of inventive step for the reasons given above in respect of claim 1.

2.3 Claims 8 and 9

These claims are method claims, relating to a method of fabricating a semiconductor programmable device according to the device claim 4 or 5. Claims 8 and 9 are thus restricted to the fabrication of a specific device as defined in claim 4 or 5, respectively, and the device produced by the claimed method must therefore, in the Board's view, comprise all the features of the claim to which they refer. This is the case despite the fact that the method claims do not specify all the steps necessary

for producing the device. Since claims 4 and 5 are considered to involve an inventive step, claims 8 and 9 also comply with the requirement of inventive step.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent with description, claims and drawings, including the amendments, as specified in Section VI above.

The Registrar: The Chairman:

M. Beer G. D. Paterson