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DECISION
of 9 February 1994

Case Number: T 0537/92 - 3.4.1

Application Number: 86103235.7

Publication Number: 0195977

IPC: H01L 21/90

Language of the proceedings: EN

Title of invention:
Metal interconnection system with a planar surface

Applicant:
Hewlett-Packard Company

Opponent:
-

Headword:
-

Relevant legal norms:
EPC Art. 84, 123(2), 56

Keyword:
"Inventive step (yes, after amendment)"

Decisions cited:
-

Catchword:
-

Case Number: T 0537/92 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 9 February 1994

Appellant: Hewlett-Packard Company
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 14 February 1992 refusing European patent application No. 86 103 235.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G.D. Paterson
Members: H.J. Reich
R.K. Shukla

Summary of Facts and Submissions

I. European patent application No. 86 103 235.7 (publication No. 0 195 977) was refused by a decision of the Examining Division.

II. The reason given for the refusal was that the subject-matter of Claim 1 filed on 13 November 1991 did not satisfy the requirements of Articles 52 and 56 EPC having regard to documents:

D2: EP-A-0 046 525, and
D3: Conference papers of the "International Electron Devices Meeting 1983), Washington, 5 to 7 December 1983, pages 550 to 553, IEEE, New York.

The Examining Division took the following view:

The process for forming a multilayer integrated circuit disclosed in document D3 would, *inter alia*, comprise the claimed step of depositing a second dielectric layer of SiO_2 on the surface of the first dielectric layer **and the tungsten.** Hence, a skilled person would arrive at the essential features claimed in Claim 1 by replacing the conventional SiO_2 of the first and second dielectric layer by polyimide. Document D3 would teach that selective chemical vapour deposition (CVD) of tungsten requires nucleation sites as catalytical activators which can be formed by surface damages resulting from sputter or plasma processes. This "activation" method is also applied in the process claimed. The skilled person who is aware of the good thermal mechanical and electrical properties of polyimides and of their ability to planarize underlying topographical features as disclosed in document D2, would automatically be led to try the described method substituting polyimide for

silicon oxide, because a process engineer would at least strongly suspect the polyimide to behave like SiO_2 and to form nucleation sites when having a physically damaged surface.

III. The Appellant lodged an appeal against this decision, requesting grant on the basis of Claim 1 filed on 17 January 1991 (the wording of the claim not specifying the material of dielectric layers) as main request, and grant on the basis of Claim 1 filed on 13 November 1991 (restricted to dielectric layers of polyimide) and forming the basis of the decision under appeal, as an auxiliary request. In support of an inventive step in the subject-matter of Claim 1 of his main request the Appellant argued mainly that none of the prior art documents, including document D3, teaches to activate a dielectric layer **surface** in selected regions for selective CVD growth of tungsten but each of them teaches to remove any nucleation sites from the dielectric layer surface and to grow tungsten only on the bottom of a via on either pure silicon or metal. Moreover, with regard to Claim 1 of the auxiliary request, there is not even any mention in document D3 of using polyimide as dielectric for selectively growing tungsten in a process for achieving a planar metallisation.

IV. In a communication pursuant to Article 110(2) EPC the Board informed the Appellant of its preliminary view that Claim 1 according to the main request was not allowable pursuant to Article 123(2), and that a new Claim 1 amended with a view to overcoming the Article 123(2) objection would not be allowable under Article 56 EPC. Against Claim 1 according to the auxiliary request the Board raised a series of objections under Articles 84 and 123(2) EPC. In particular, it was pointed out that the auxiliarily

requested wording of Claim 1 apparently did not clearly define an essential feature of the invention disclosed in the description of the application, page 9, paragraph 1, namely that - in contrast to the disclosure in the nearest prior art document D3 - not only the vias but **also the interconnecting lines** are formed by selective CVD of tungsten.

V. In response to this communication the Appellant filed on 14 October 1993, as main request, an amended Claim 1 in order to overcome the objections raised by the Board, and requested that the decision under appeal be set aside and that a patent be granted on the basis of the following documents:

Claims: 1 to 3 filed on 14 October 1993 with letter dated 12 October 1993;

Description: pages 1 to 7, 11, 14 and 18 according to EP-A-0 195 977, and pages 8, 8a, 8b, 9, 10, 12, 13, 15, 16, 17 and 19 filed on 14 October 1993 with letter dated 12 October 1993;

and with the amendments in Claims 1, 2 and on page 8b as requested during a consultation by telephone on 16 December 1993 and 5 February 1994;

Drawings: sheets 1/10 to 10/10 according to EP-A-0 195 977.

VI. Independent Claim 1 reads as follows:

"1. A process for forming a multilayer integrated circuit having substantially planarized layers of dielectric and tungsten conductors comprising the steps of: depositing a first polyimide layer on a substantially non-planarized surface of said integrated circuit to form a first substantially planarized surface; forming a first mask over said first polyimide

surface in a first predetermined pattern to expose portions of said first substantially planarized surface to be etched; selectively removing portions of said first polyimide layer corresponding to said first predetermined pattern formed by said first mask using an etchant whereby said etchant activates etched surfaces of said first polyimide layer by damaging said etched surfaces of said first polyimide layer to initiate the growth of tungsten on said etched surfaces; removing said first mask from said first polyimide surface; growing tungsten on said etched surfaces using chemical vapor deposition techniques until said tungsten substantially fills said selectively removed portions of said first polyimide layer and the surface of the deposited tungsten becomes approximately level with said first substantially planarized surface of said first polyimide layer; depositing a second polyimide layer on said first substantially planarized surface consisting of said first polyimide layer and of deposited tungsten to form a second substantially planarized surface; forming a second mask over said second substantially planarized surface in a second predetermined pattern to expose portions of said second substantially planarized surface to be etched; selectively removing portions of said second polyimide layer corresponding to said second predetermined pattern formed by said second mask to form vias and trenches for interconnecting lines to be formed, exposing thus portions of the first substantially planarized surface using an etchant whereby said etchant activates etched surfaces of said first and second polyimide layer by damaging said etched surfaces of said first and second polyimide layer to initiate the growth of tungsten on said etched surfaces of said first and second polyimide layer; removing said second mask from said second polyimide layer; and growing tungsten on etched surfaces of said first and second polyimide layer using chemical vapor deposition

techniques until said tungsten substantially fills said selectively removed portions of said second polyimide layer and the surface of the deposited tungsten becomes approximately level with said second substantially planarized surface of said second polyimide layer."

Claims 2 and 3 are dependent on Claim 1.

Reasons for the Decision

1. Claim 1 comprises the subject-matter of original Claims 1, 2, 4, 6, 9 and features disclosed in the original description page 12, paragraph 3; page 13, paragraph 2; page 15, paragraph 2; page 16, paragraph 3; page 17, paragraph 1 and 2; page 18, paragraph 1 in combination with Figures 2 to 7. The subject-matter of Claim 2 is disclosed in Figures 8 to 10 and the corresponding description. The subject-matter of Claim 3 is disclosed in the original description page 15, paragraph 2 to page 16, paragraph 1. The amendments of the description are in compliance with Rules 27(1)(b) and (c) EPC. There is, therefore, no objection under Article 123(2) EPC to the current set of application documents.

2. *Novelty*

2.1 Document D3 discloses, in the wording of the one-part form of Claim 1:

"A process for forming a multilayer integrated circuit having substantially planarized layers of dielectric and tungsten conductors comprising the steps of: depositing a first "silicon dioxide" layer on a substantially non-planarized surface of said integrated circuit to form a

first ... surface; forming a first mask on said first "silicon dioxide" surface in a first predetermined pattern to expose portions of said first ... surface to be etched; selectively removing portions of said first "silicon dioxide" layer corresponding to said first predetermined pattern formed by said first mask using an etchant whereby said etchant activates etched surfaces of said first "silicon dioxide" layer ... to initiate the growth of tungsten on said etched surfaces; removing said first mask from said first "silicon dioxide" surface (see D3, page 553, Fig. 7, step 1 in combination with page 551, left column, lines 31-34 and right column, line 31); growing tungsten on said etched surfaces using chemical vapor deposition techniques (D3, Fig. 7, step 2 in combination with page 551, right column, lines 34 and 35); ... depositing a second "silicon dioxide" layer on said first ... surface to form a second surface; forming a second mask on said second ... surface in a second predetermined pattern to expose portions of said second ... surface to be etched; selectively removing portions of said second "silicon dioxide" layer corresponding to said second predetermined pattern formed by said second mask ... using an etchant whereby said etchant activates etched surfaces of said second "silicon dioxide" layer ... to initiate the growth of tungsten on said etched surfaces of said ... second "silicon dioxide" layer (Fig. 7, step 4) and growing tungsten on said etched surfaces of said ... second "silicon dioxide" layer using chemical vapor deposition techniques ... (Fig. 7, step 5)."

2.2 The prior art device according to document D3 uses silicon dioxide instead of the claimed polyimide as material for the first and second dielectric layers and forms the trenches for the interconnecting lines between the dielectric by conventional subtractive etching of an $MoSi_2$/Al-Si alloy instead of the claimed additive

selective deposition of tungsten on predetermined polyimide surface regions activated by etch-produced surface damages. The remaining documents cited in the European Search Report under Article 54(2) EPC do not come closer to the subject-matter of Claim 1. In the process disclosed in document EP-A-0 156 999 (D1) cited under Article 54(3) EPC, silicon dioxide is used as a dielectric.

2.3 Thus, the subject-matter of Claim 1 is considered novel in the sense of Article 54 EPC.

3. *Inventive step*

3.1 Starting from the closest prior art according to document D3, the objective problem underlying the present invention is to provide a process which is essentially planar, avoids shorts and opens in the interconnecting conductor lines and offers higher adhesion between the interconnecting conductor lines and the dielectric surfaces; see the description, page 9, paragraphs 2 and 3.

3.2 The problem is solved in that:

(a) the conventional dioxide of the first and second dielectric layers is replaced by "polyimide";

(b) the activation of the dielectric layer surfaces to initiate the growth of tungsten is effected by "damaging" the polyimide layer surface;

(c) tungsten is grown "until said tungsten substantially fills said selectively removed portions of said first polyimide layer and the surface of the deposited tungsten becomes

approximately **level** with said first substantially planarized surface of said first polyimide layer"; and

(d) said second polyimide layer is removed "to form vias **and trenches for interconnecting lines**, exposing thus portions of the first substantially planarized surface; ... damaging said etched surfaces of said **first** and second polyimide layer" to initiate the growth of tungsten and growing tungsten on etched surfaces of said "**first** and second polyimide layer ... until said tungsten substantially fills said selectively removed portions of said second polyimide layer and the surface of the deposited tungsten becomes approximately level with said second substantially planarized surface of said second polyimide layer.

The avoidance of opens and shorts in the interconnecting lines results from two measures: The use of the first polyimide layer according to measure (a), which as a spin-on polymer tends to planarise the resulting layer surfaces, compensates discontinuities in the surface of the integrated circuit. Step (d) eliminates any underetching or overetching of the conventional subtractive technique. The improvement of adhesion results from the deposition of conductor into a trench of the polyimide layer according to measure (d). This tungsten deposition results in more contact area between conductor and dielectric; see also the description page 10, paragraph 3.

3.3 Document D3 employs the selective chemical vapour deposition of tungsten in order to fill out contact windows to the silicon wafer and via holes between higher metallisation levels. However, the interconnecting lines in each metallisation level are

formed by depositing a homogenous layer of a different conductor material on top of a more or less planarized tungsten and dielectric surface and by etching the homogenous layer in a subtractive process. In document D2, contact windows, vias and interconnecting lines all are produced by a subtractive technique. The conductive material in each level is evaporated upon a patterned double layer of polyimide and polysulfon to such an extent that the conductor fills the openings in the polyimide layer and overlies the surface of the polysulfon layer. Thereafter the polysulfon layer with the overlying conductor is etched away (lift-off technology). The remaining ESR-documents cited under Article 54(2) EPC do not describe processes for forming multilayer metallisations of integrated circuits.

3.4 Hence, in the Board's view, having regard to the cited prior art, it is not obvious for a skilled person to improve the adherence of conductor and dielectric in a multilayer integrated circuit by the selective chemical vapour deposition of tungsten into vias **and** trenches for interconnecting lines, offering thus a larger contact area; see also paragraph 3.2 above. For this reason measure (d) as set out in paragraph 3.2 above is considered to be the result of an inventive step.

3.5 Therefore, the question whether a skilled person is able to foresee that polyimide, disclosed in document D2 as a dielectric frame surrounding an evaporated conductor metal, can be transformed by etching into an activated surface enabling the selective CVD of tungsten, can be left open, see paragraph II above.

3.6 For the reasons indicated in paragraphs 3.1 to 3.4, the subject-matter of Claim 1 is considered to involve an inventive step in the sense of Article 56 EPC.

4. Thus, Claim 1 is allowable under Article 52(1) EPC. Dependent Claims 2 and 3 concern particular embodiments of the device claimed in Claim 1 and are, therefore, likewise allowable.

Order

For these reasons, it is decided that:

1. The decision of the Examining Division is set aside.

2. The case is remitted to the first instance in order to grant a patent on the basis of the following documents:

Claims: 1 to 3 filed on 14 October 1993;
Description: pages 1 to 7, 11, 14 and 18 according to EP-A-0 195 977;
pages 8, 8a, 8b, 9, 10, 12, 13, 15, 16, 17 and 19 filed on 14 October 1993
and with the amendments in Claims 1, 2 and on page 8b as requested on 16 December 1993 and 5 February 1994;
Drawings: sheets 1/10 to 10/10 according to EP-A-0 195 977.

The Registrar: The Chairman:

M. Beer G.D. Paterson