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D E C I S I O N
of 28 September 1995

Case Number: T 0680/92 - 3.4.1

Application Number: 87304812.8

Publication Number: 0249371

IPC: H01L 29/203

Language of the proceedings: EN

Title of invention:
Semiconductor device including two compound semiconductors, and method of manufacturing such a device

Applicant:
HITACHI, LTD.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54, 56

Keyword:
"Novelty and inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0680/92 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 28 September 1995

Appellant: HITACHI, LTD.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 10 March 1992 refusing European patent application No. 87 304 812.8 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. D. Paterson
Members: J. H. Reich
Y. J. F. van Henden

Summary of Facts and Submissions

I. European patent application No. 87 304 812.8 (publication No. 0 249 371) was refused by a decision of the Examining Division.

II. The reason given for the refusal was that Claim 1 of the main request filed 6 November 1991 did not satisfy Article 54(2) EPC with regard to document:

D1: Inst. Phys. Conf. Ser., No. 74, chapter 5, 1985; paper presented at Int. Symp. GaAs and Related Compounds, Biarritz 1984, pages 321 to 326.

The Examining Division took the view the prior art device disclosed in document D1, page 325, paragraph 2.2 (wherein the obvious error "80Å AlAs" in Figure 6 was interpreted as 80Å AlGaAs in the light of the text on page 325, lines 5 to 10) fell within the scope of Claim 1. The Applicant's argument that in view of the experimental findings in document:

B: C. H. L. Goodman "Crystal Growth", volume 2, Plenum Publishing Corporation, 1978, pages 1 and 10 to 13,

there were in the prior art device according to document D1 absolutely no mismatch dislocations was "not accepted" by the Examining Division.

III. The Applicant lodged an appeal against this decision. In the Statement of Grounds of Appeal the main request was to maintain the claimed subject-matter unamended, and an auxiliary request was also filed. Furthermore, oral proceedings were requested auxiliarily. In order to support its case the Appellant referred to documents:

A: Applied Physics Letters, volume 47, number 3, 1985, pages 322 to 324; and Erratum, **ibid**, volume 49, number 4, 1986, page 229;

C: Japanese Journal of Applied Physics, volume 30, number 3B, 1991 pages 447 to 450

and cited for the first time documents:

E: IEEE Journal of Quantum Electronics, volume QE-11, number 7, 1975, pages 562 to 568;

F: Journal of Applied Physics, volume 47, number 7, 1976, pages 3374 to 3376;

G: Applied Physics Letters, volume 52, number 7, 1988, pages 543 to 545; and

H: Journal of Applied Physics, volume 62, number 4, 1987, pages 1212 to 1219.

IV. In support of his main request the Appellant argued essentially as follows:

(a) Claim 1 is novel, since - despite the apparent lattice mismatch in document D1 - there are no misfit dislocations in this device. In document B the surprising finding that an AlGaAs layer grows on a GaAs substrate free of dislocations, is explained by no misfit between the lattices at deposition temperature and by only small sheer strains at cooling which strains are insufficient to cause dislocations. Furthermore, a comparison with explicit values of the critical layer thickness (below which no dislocations are produced by a lattice mismatch) as disclosed in document A shows that the thickness of the relevant layer in

document D1 is below the critical layer thickness for dislocations. The Examining Division contradicted knowledge in the art without any documentary support for its finding that the conclusions of the skilled writers of documents A and B are invalid.

(b) Assuming that the device disclosed in Figure 6 of document D1 had dislocations in the 80Å AlGaAs-layer, they would not be inactivated by the conventional Si dopant plane, since this plane is disclosed to form an "atomic plane", which normally has a discontinuous series of atoms. In the event that a dislocation happens to coincide with a gap between the dopant atoms, no inactivation occurs. Thus, document D1 does not show a layer of impurities sufficient to inactivate dislocations like the invention. This fact is supported independently by document C.

(c) Starting from document D1 as the closest prior art, the problem would be to inactivate dislocations in a device with greater lattice-mismatching than that in the device of document D1. In such a modified device the conventional atomic plane of dopant would not perform the required function of inactivating dislocations. In these circumstances it may seem preferable to consider as closest prior art that disclosed in the documents cited in the description page 2, lines 1 to 18, i.e.:

D2: IEEE Electron Device Letters, volume EDL-6, 1985, pages 20 and 21, and

D3: Applied Physics Letters, volume 46, 1985, page 1145.

In either case, no evidence has been produced, that it was known in the art to inactivate dislocations due to lattice mismatch by an impurity layer. Documents E, F, G and H evidence that electrical neutralisation by impurities results in physical blocking of misfit dislocations. Such effect is nowhere disclosed in the prior art.

V. In a communication pursuant to Article 110(2) EPC the Board expressed its preliminary view essentially as follows:

(a) The Board does not accept the opinion of the first instance that document D1 anticipates Claim 1 of the present main and auxiliary requests.

(b) However, Claims 1 and 9 of the main and auxiliary requests do not satisfy Article 123(2) EPC, since the original description does not disclose "dislocations" but dislocation networks. Moreover, there would be no disclosure of "dislocations" (or a high density of dislocation networks) in the second compound semiconductor region (41, 42, 43). but only in the first GaAs layer (41). Furthermore, a skilled reader cannot derive from the original documents "...impurities which are **sufficient** to inactivate...", in the sense that only one impurity layer with an adequate quantity of impurities is able to **completely** eliminate energy band bending (Figures 5(a) and 5(b) or in that a threshold quality is necessary for the inactivation process.

(c) In order to satisfy Article 84 EPC it appeared necessary to include in Claims 1 and 9 a functional definition of the **type** of impurity, capable of eliminating leakage current-producing energy band bending; to exclude blind tunnel currents

(Figure 4(a) and (b)) caused by excessive doping of the impurity layers via a functional definition of the upper limit of the impurity concentration combined with the appropriate thickness of the second compound layer (41, 43) for avoidance of tunnel currents; to clarify that the "at least two semiconductor layers (41, 43)" are **second compound** semiconductor layers; and to express more clearly that the "at least one impurity layer (42)" shall be present between each couple of adjacent second compound semiconductor layers in view of the embodiments disclosed.

VI. In reply to the Board's communication and following a consultation by telephone with the Rapporteur, the Appellant requested that a patent be granted on the basis of the following text:

Claims: 1 to 10 filed 4 August 1995 with letter dated 2 August 1995;

Description: Original pages 1, 4, 5, 7 to 10, pages 2, 3, 3a, 3b filed 4 August 1995 with letter dated 2 August 1995, pages 6 and 11 filed 4 December 1991 with letter dated 28 November 1991;

Drawings: original sheet 1/2 and 2/2;

and with the amendments of clerical errors on pages 2, 3, 3b and in Claims 7, 8 and 9 as requested on 14 September 1995.

VII. Independent Claims 1 and 9 read as follows:

"1. A semiconductor device having a first compound semiconductor region (3) with a first lattice constant, and a second compound semiconductor region (41,42,43) on the first compound semiconductor region (3), with a second lattice constant different from the first lattice constant;

the second compound semiconductor region (41,42,43) having at least two second compound semiconductor layers (41,43) and there being at least one impurity layer (42) between adjacent second compound semiconductor layers (41,43) of the second compound semiconductor region (41,42,43) respectively;

characterised in that:

the first and second lattice constants of the first and second compound semiconductor regions (3;41,42,43) differ such that the lattice mismatch thereof causes dislocation networks in the second compound semiconductor layers (41) neighbouring the first compound semiconductor region (3); in that the at least one impurity layers (42) has impurities which are selectively adsorbed or gettered around the dislocations and of such a type that they neutralize the resulting charges of the dislocation cores; and in that the impurity concentration in the at least one impurity layer (42) is adapted to the thickness of the second compound semiconductor layers (41,43) such that tunnel currents through the second semiconductor region (41,42,43) are avoided.

9. A method of manufacturing a semiconductor device comprising forming a first semiconductor layer (41) on a first compound semiconductor region (3) which has a first lattice constant, the first semiconductor layer (41) being a second compound semiconductor with a second lattice constant different from the first lattice constant; forming at least one impurity layer (42) on the first compound semiconductor layer (41); and

forming a second semiconductor layer (43) of the second compound semiconductor over the at least one impurity layer (42);

characterised in that:

the first and second lattice constants differ such that the mismatch thereof causes dislocation networks in the first semiconductor layer (4); and the at least one impurity layer (42) has impurities which are selectively adsorbed or gettered around the dislocations and of such type that they neutralize the resulting charges of the dislocation cores; and in that the impurity concentration in the at least one impurity layer (42) is adapted to the thickness of the second compound semiconductor layers (41,43) such that tunnel currents through the second semiconductor region (41,42,43) are avoided."

Claims 2 to 8 are dependent on Claim 1 and Claim 10 is dependent on Claim 9.

Reasons for the Decision

1. The subject-matter of Claims 1 and 9 comprises the subject-matter of original Claims 1 and 9 respectively and features disclosed in the description; page 2, line 1 to page 3, line 13; page 4, lines 24 to 27; page 8, lines 6 to 14; and page 8, line 26 to page 9, line 3. The subject-matter of Claim 2 is disclosed in the description page 6, lines 6 to 8. Claims 3 to 8 and 10 correspond to original Claims 3 to 8 and 10 respectively.

2. *Novelty - Claims 1 and 9*

2.1 The pre-characterising part of Claim 9 comprises method steps which are defined by measures resulting in the structural features claimed in the pre-characterising part of Claim 1. As agreed to by the Appellant, a device having the features defined in the pre-characterising part of Claim 1 and a method with the steps defined in the pre-characterising part of Claim 9 are both disclosed in document D1, see the introductory part of the description. The almost identically worded characterising parts of Claims 1 and 9 concern the same properties of the claimed semiconductor structure. For these reasons, novelty and inventive step of Claims 1 and 9 can be assessed together.

2.2 Having regard to the crucial question whether document D1 discloses to a skilled person that the conventional second compound semiconductor region (see 80Å AlAs-layer neighbouring 1.0µm GaAs layer in Figure 6 of document D1) is free of dislocations, the Board sees no reason to doubt the experimental results disclosed in document B, page 11, paragraph 2 to page 12, paragraph 2 in combination with Figures 8 and 9, that a $2 \cdot 10^3$ nm

thick AlAs-layer and a $1 \cdot 10^3$ nm AlGaAs layer show no interfacial misfit dislocations in a reflection X-ray topography. The comparable Al(Ga)As-layer of document D1 is an order of magnitude thinner and has only a thickness of $1.6 \cdot 10^2$ nm. Having regard to the known appearance of a critical layer thickness above which dislocations form (see for instance document A), in the Board's view a skilled person would conclude that if in a 1000 nm thick-layer no misfit dislocations can be observed in a X-ray reflection topography, the same or even a better experimental result can be expected for a 160 nm thick layer.

2.3 In the Board's view, there is therefore no evidential basis on which it would be reasonable to assume the presence of dislocations in the structures according to documents B and D1.

2.4 Furthermore, document D1 is silent about the neutralisation of charges of dislocations by impurities, and about an adaption of the impurity concentration to the thickness of the second compound semiconductor layers for avoiding tunnel currents.

2.5 For the reasons set out in paragraphs 2.1 to 2.5 above, in the Board's judgement the subject-matter of independent Claims 1 and 9 is new in the sense of Article 54 EPC.

3. *Inventive Step - Claims 1 and 9*

3.1 The conventional impurity layer disclosed in document D1 is used as a means for increasing electron mobility within the second compound semiconductor layer; see paragraph 2.3 on page 325 and the summary on page 326. Neither document D1 nor any other cited document hints to a skilled person to getter or selectively adsorb

around dislocations an impurity of a type which neutralises the resulting charges of the dislocations. Hence, in the Board's view, it was not obvious for a skilled person to provide such impurities for the technical purpose of reducing tunnel currents, in particular not in the **L**attice **M**ismatched **G**ate-FET disclosed in Figure 1 of document D2 in order to reduce blind currents in this device.

3.2 For the above reasons, in the Board's judgement the subject-matter of independent Claims 1 and 9 involves an inventive step in the sense of Article 56 EPC.

4. Thus, independent Claims 1 and 9 satisfy Article 52(1) EPC. Claims 2 to 8 concern particular embodiments of the device claimed in Claim 1. Claim 10 is directed to a particular embodiment of the method claimed in Claim 9. Therefore, Claims 2 to 8 and 10 are allowable.

Order

For these reasons it is decided that:

1. The decision of the Examining Division is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the requested text (see paragraph VI above).

The Registrar: The Chairman:

M. Beer G. D. Paterson