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D E C I S I O N
of 15 December 1995

Case Number: T 0700/92 - 3.4.1

Application Number: 87309773.7

Publication Number: 0269294

IPC: H01L 21/18

Language of the proceedings: EN

Title of invention:
Method of manufacturing a bonded structure type semiconductor substrate

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
Bonded semiconductor structure/TOSHIBA

Relevant legal provisions:
EPC Art. 56

Keyword:
"A measure disclosed to be 'conventional' in a prior art document"
"Conventional measure not an obvious choice"
"Inventive step - yes (after amendment)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0700/92 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 15 December 1995

Appellant: KABUSHIKI KAISHA TOSHIBA
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 18 March 1992 refusing European patent application No. 87 309 773.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. D. Paterson
Members: R. K. Shukla
H. J. Reich

Summary of Facts and Submissions

I. European patent application No. 87 309 773.7 was refused by a decision of the Examining Division on the ground that the subject-matter of independent claim 1 of both the main request and the auxiliary request filed on 30 November 1991 did not fulfil the requirement of Articles 52 and 56 EPC regarding inventive step.

The Examining Division referred, inter alia, to the following prior art documents in the decision:

D1- EP-A-0 192 229;

D2- Japanese Journal of Applied Physics, vol. 19, 1980, supplement 19-1, pages 61 to 64;

D3- S.M. Sze: Physics of Semiconductor Devices (2nd edition), Wiley, New York, 1981, page 32 and D5 - S.M. Sze: Physics of Semiconductor Devices (2nd edition), Wiley, New York, 1981, pages 70, 71.

II. Independent claim 1 of the above main request had the following wording:

"A method of manufacturing a bonded structure type semiconductor substrate, comprising the steps of ion-implanting phosphorus into a first semiconductor substrate (1) of n-type conductivity to form an n-type ion-implanted layer (2) in a surface region of said first semiconductor substrate (1); causing said first semiconductor substrate (1) to be subjected to a first thermal treatment; bonding a p-type surface of a second p-type semiconductor substrate (3) to the n-type surface of said ion-implanted layer, and performing a second thermal treatment after said first and second semi-conductor substrates have been bonded, characterized in that the ion-implantation is carried out at a dose of

more than 5 x 10^{14} atom/cm^2, in that the first thermal treatment on the first semiconductor substrate is within the temperature range of 600°-1200°C, to decrease the concentration of phosphorus in the surface portion of the ion-implanted layer, and in that the second semiconductor substrate has a specific resistance of not more than 0.05 ohm cm."

Independent claim 1 of the auxiliary request differed from the above claim in that the temperature range of the first thermal treatment was 1000° to 1200°C.

III. In its decision, the Examining Division held essentially as follows.

Document D1, which constitutes the closest prior art, discloses all the features of claim 1 of the main request except the features specifying that:

(a) the implantation dose of phosphorus is more than 5 x 10^{14} atom/cm^2;

(b) the temperature of the first thermal treatment is between 600 and 1200°C; and

(c) the first thermal treatment is done in order to decrease the concentration of phosphorus in the surface portion of the ion-implanted layer.

Although the exact nature of the first thermal treatment is not disclosed in document D1, a skilled person would regard thermal treatment subsequent to ion implantation in this document as referring to a conventional annealing step well known per se in the art, which as shown by document D2 involves a thermal treatment at 1100°C, that is, at a temperature between 600°C and 1200°C. Also, as is evident from document D2, an

implantation dose of phosphorus ions in the range of 1 to 3 x 10^{16} cm^{-2} is required to produce a highly doped n+ region in silicon, so that the ion implantation dose of phosphorus as specified in claim 1 under consideration would be obvious to the skilled person. Moreover, an annealing step such as disclosed in document D2 necessarily entails redistribution of implanted ions and a decrease in its surface concentration. As the depth of implanted phosphorus ions in silicon is known from document D5 to lie between 0.01 and 0.3 micron and since the thickness of the phosphorus implanted n+ layer in document D1 following annealing is disclosed to be between 5 and 30 micron, it is implicit in document D1 that the annealing step is carried out for redistributing implanted phosphorus.

The same reasons also apply to claim 1 of the auxiliary request, since the temperature for the thermal treatment suggested in document D2 (1100°C) also falls within the range claimed in claim 1 of the auxiliary request.

IV. The Applicant lodged an appeal against the decision and filed experimental evidence submitted by Mr Tadahide Hoshi, the inventor, to demonstrate the effect of doping concentration on the formation of microvoids at the interface of a bonded type substrate. The Applicant submitted essentially the following arguments in the statement of grounds of appeal.

Typical implantation doses of phosphorus ions for producing n-type layer extend both above and below the dosage 5 x 10^{14} $atom/cm^2$. The selection of the upper range according to the present invention contributes to an inventive step since as shown by the experimental results submitted by the inventor, Mr Tadahide Hoshi,

microvoid defects in the bonding area become a problem only when the ion implantation dose is 5×10^{14} or higher.

Concerning the first thermal treatment, it is stated in document D1 that "the resultant structure is heat treated to form N+ type silicon layer 32" (page 6, lines 34 to 35). This passage must be interpreted to refer to any heat treatment sufficient to establish an n+ type silicon layer. There is thus no indication in document D1 that this heat treatment should be an annealing treatment in the temperature range claimed in the present invention. This interpretation is supported by the fact that in the embodiment described in connection with Figure 5 in document D1 no "first thermal treatment" is mentioned.

V. In a communication pursuant to Article 110(2) EPC, the Board cited the following pages of a text book as evidence of the common general knowledge in the field of annealing subsequent to ion implantation :

D6- S.M. Sze: Semiconductor Devices - Physics and technology, John Wiley and Sons, 1985, pages 417 to 420.

In the communication the Appellant was informed that having regard to document D1 and what was common general knowledge, the subject-matter of claim 1 of the Appellant's main request, in so far as it involved a thermal treatment at a temperature between 600°C and 800°C for an ion implantation dose of phosphorus above 5×10^{14} cm^{-2} did not appear to involve an inventive step.

The Appellant was also informed that a thermal treatment at a temperature between 1000°C and 1200°C as in claim 1 of the auxiliary request was not rendered obvious by what was disclosed in document D6.

VI. In response to the above communication, the Appellant filed new claims 1 to 4 with a letter dated 6 January 1995, forming the basis of his only request for the grant of a patent. In a consultation by telephone with the Rapporteur on 23 October 1995, the Appellant requested that claim 1 be changed to the one-part form by substituting the expression "characterized in that" by "wherein".

Independent claim 1 has the following wording:

"A method of manufacturing a bonded structure type semiconductor substrate, comprising the steps of ion-implanting phosphorus into a first semiconductor substrate (1) of n-type conductivity, to form an n-type ion-implanted layer (2) in a surface region of said first semiconductor substrate (1); causing said first semiconductor substrate (1) to be subjected to a first thermal treatment; bonding a p-type surface of a second p-type semiconductor substrate (3) to the n-type surface of said ion-implanted layer, and performing a second thermal treatment after the first and second semi-conductor substrates have been bonded, wherein the ion-implantation is carried out at a dose of more than 5×10^{14} atom/cm^2, where in the first thermal treatment on the first semiconductor substrate is within the temperature range of 1000° - 1200°C, to decrease the concentration of phosphorus in the surface portion of the ion-implanted layer and to reduce or prevent formation of microvoids at the interface of the bonded semiconductor substrates (1,3), and where in the second

semiconductor substrate has a specific resistance of not more than 0.05 ohm cm."

Reasons for the Decision

1. The Board is satisfied that the amended claims fulfil the requirement of Article 123(2) EPC.

In the present appeal, the only issue under dispute is that of inventive step.

2. *Inventive step*

2.1 Document D1, which constitutes the closest prior art, discloses (see in particular page 6, line 12 to page 7, line 32 and Figure 4) a method of manufacturing a bonded structure type semiconductor substrate, comprising the steps of ion-implanting phosphorus into a first semiconductor substrate (31) of n-type conductivity and subjecting the first semiconductor substrate to a first thermal treatment to form an n+ -type ion-implanted layer (32) in a surface region of the first semiconductor substrate (31) (see page 6, lines 31 to 33); bonding a p-type surface of a second p-type semiconductor substrate (33) to the n-type surface of said ion-implanted layer by subjecting the assembly of the first and second semiconductor substrate to a second thermal treatment at a temperature above 200°C (see page 7, lines 26 to 32). Furthermore, the p-type substrate 33 has a boron concentration of between 10^{19} and 10^{21} cm^{-3} (page 6, line 37), which according to a standard textbook (see document D3, Figure 21) corresponds to a substrate resistivity , that is, specific resistance between 0.01 and 0.0001 ohm cm.

Hence, it is implicit in document D1 that the second semiconductor substrate has a specific resistance less than 0.05 ohm cm.

Document D1 however does not specify the ion-implantation dose of phosphorus nor does it specify the temperature used for the first thermal treatment.

2.2 The claimed subject-matter is thus distinguished over the prior art disclosed in document D1 in that the phosphorus ion-implantation in the first substrate is carried out at a dose of more than 5×10^{14} atom/cm^2 and the first thermal treatment on the first semiconductor substrate is within the temperature range of 1000° - 1200°C so as to decrease the concentration of phosphorus in the surface portion of the ion-implanted layer and to reduce or prevent formation of microvoids at the interface of the bonded semiconductor substrates.

2.3 According to the description in the application as filed (see column 4, lines 35 to 40 of the published application) and as shown by the results of the experiments submitted by the Appellant, the formation of microvoids at the junction of the bonded structure takes place only when the ion implantation dose of phosphorus is greater than 5×10^{14} atom/cm^2. Although the Board accepts that the ion implantation dose of phosphorus is critical in the formation of microvoid defects, as shown by the disclosure in document D2 (see page 61) the above specified dose phosphorus is typically employed in the art to produce a highly doped region of n-conductivity type. Moreover, this detrimental effect (the microvoid formation) of a relatively high dose of phosphorus was not known in the art prior to the filing of the present application, so that a skilled person had no reason to refrain from employing such a typical implantation dose of phosphorus in the method according to document D1. In

the Board's view therefore the phosphorus implantation dose as specified in claim 1 under consideration would have been routinely employed by the skilled person in the method disclosed in document D1.

2.4

2.4.1 As regards the first thermal treatment subsequent to an ion implantation step, referred to in document D1 on page 6, lines 34 to 35, the Board agrees with the Examining Division that a skilled person would regard this as referring to an annealing treatment which is well known in the field of semiconductor device technology and which necessarily follows ion implantation in order to activate the implanted ions and restore mobility and life time.

A skilled person looking for information about annealing temperatures to be employed in the method according to document D1 would consult document D6 (which is a standard textbook on semiconductor device technology), in particular, Section 10.5.2 on pages 417 and 418, where annealing behaviour of phosphorus implantation into silicon is described (see Figure 30 and the corresponding description on page 418, first paragraph). It is evident from this disclosure that for a phosphorus ion-implantation dose in silicon of between 5×10^{14} and about 10^{15} per cm^2, annealing at around 800°C is required to activate the implanted ions, and for implantation doses higher than 10^{15} per cm^2, the required annealing temperature is about 600°C. The required annealing temperature according to what is to be regarded as common general knowledge is thus not higher than 800°C.

Concerning the temperature to be employed in the annealing step, i.e the first heat treatment, in the method of document D1, the Examining Division relied on

a single statement in document D2 (see page 61, right hand column, third paragraph) which reads, "For comparison, conventional single-stage annealing in dry nitrogen at a temperature above 1100°C was carried out". In the Board's view, this statement (even when it is interpreted to mean that the term "conventional" qualifies both the single-stage annealing and the temperature of 1100°C) is to be read in the context of, inter alia, the "Conclusions" in document D2. It is disclosed there that the first stage low-temperature (which according to page 61, right-hand column, paragraph 3 is between 700°C and 1000°C) wet-oxygen oxidation removes the surface defects formed by implantation and that this surface defect removal might be considered as a possible cause of noise performance improvement. The second stage of annealing disclosed in document D2 involves dry nitrogen annealing at 1200°C for base drive-in and at 1100°C for emitter drive-in. The above mentioned single stage annealing at temperatures above 1100°C was used in document D2 merely as a comparative test to demonstrate the advantages of the proposed two-stage annealing, and does not remove surface defects. Hence in the Board's view, the skilled person learns from document D2 that the annealing process at a temperature of 1100°C is unlikely to produce a satisfactory semiconductor structure. Document D2 therefore does not provide any incentive to a skilled person to employ such a high annealing temperature.

In view of the above, in the present case choice of 1100°C as annealing temperature does not represent an obvious choice which the skilled person would have made having regard to the disclosure in document D2 taken as a whole and the common general knowledge as shown by document D6.

2.4.2 The technical problem underlying the present invention consists in reducing or preventing formation of microvoid defects at a bonding interface (see column 2, lines 49 to 52 of the published application). The cited prior art documents, in particular documents D1 and D2, do not mention this problem nor do they suggest any measure to suppress the formation of microvoids. In the Board's view a skilled person is unable to foresee that for an ion-implantation dose of phosphorus as specified in the claim, the temperature range of between 1000°C and 1200°C would reduce the formation of microvoids at a bonding interface. In other words, this effect is surprising. Therefore, the claimed temperature range of first heat treatment for the ion implantation dose as specified in the claim would not be obvious to the skilled person.

2.5 For these reasons, in the Board's judgement, the subject-matter of independent claim 1 involves an inventive step within the meaning of Article 56 EPC.

Claims 2 to 4 are dependent claims and, therefore, fulfil the requirement of inventive step.

3. The description as filed needs to be amended for conformity with the claimed subject-matter in order to comply with the requirement of Rule 27(1)(c) EPC. In connection with these amendments, the Board observes that the claimed invention is now limited to a method where phosphorus is implanted into a substrate of n-type conductivity to form an n-type ion-implanted layer, which is then bonded to a second p-type semiconductor substrate. Moreover, the first thermal treatment in claim 1 is restricted to a temperature range of 1000°C to 1200°C with a view to reducing or preventing formation of microvoids at the bonding interface.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to prosecute the application further with a view to adapting the description to the subject-matter as claimed in claims 1 to 4 filed with the letter dated 6 January 1995, with the amendment to claim 1 as agreed in the telephone conversation on 23 October 1995, and grant a patent on the basis of these claims.

The Registrar: The Chairman:

M. Beer G. D. Paterson