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File Number: T 748/92 - 3.5.1

Application No.: 83 100 649.9

Publication No.: 0 085 386

Title of invention: Semiconductor device with spare memory cells

Classification: G06F 11/20

D E C I S I O N
of 7 April 1993

Applicant: KABUSHIKI KAISHA TOSHIBA

Headword:

EPC Article 56

Keyword: "Inventive step (yes)"



Case Number : T 748/92 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 7 April 1993

Appellant :

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Decision under appeal :

Decision of the Examining Division of the
European Patent Office dated 3 April 1992
refusing European patent application
No. 83 100 649.9 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : R. Randes
G. Davies

Summary of Facts and Submissions

- I. The Appellant's European patent application No. 83 100 649.9, filed on 25 January 1983, claiming priority from a previous application in Japan dated 29 January 1982, was refused by a decision of the Examining Division dated 3 April 1992.

Claim 1 filed on 10 October 1991 as refused reads as follows:

"A semiconductor memory device comprising:

- a plurality of bit-memory sections (BMS-1 to BMS-N), each bit-memory section having a plurality of memory cells arranged on a plurality of memory columns;
- a plurality of column select circuits (14-1 to 14-n), each column select circuit being coupled with said bit-memory sections;
- a plurality of spare bit-memory sections (SMS-1, SMS-2), each spare bit-memory section having spare memory cells of one column;
- control means (16-1, 16-2) being programmable to turn on switching means (36, 38) in response to column signal generated by burn-out of a fuse and specifying the column including a defect memory cell; and
- address designating circuit (34) for designating an address of the column;

characterized in that:

- said switching means (36, 38) is coupled with said spare bit-memory sections (SMS-1, SMS-2), and a further switching means (20-1 to 20-n) is provided to disconnect one or more defective bit-memory sections;

- said control means (16-1, 16-2) is programmable to turn off said further switching means (20-1 to 20-n) so as to disconnect one or more defective bit-memory sections (SMS-1, SMS-2), and at the same time, to turn on said switching means (36, 38) in response to said column signal for selecting columns of said spare bit-memory sections (SMS-1, SMS-2), so that one or more defective bit-memory sections are replaced with the spare bit-memory sections (SMS-1, SMS-2), when defective memory cells occur in a bit-memory section; and
- said control means (16-1, 16-2) includes a plurality of logic circuits (38-1 to 38-i) whose output terminals are each connected to a corresponding one of said further switching means (20-1 to 20-n), a plurality of spare signal generating circuits (32-1 to 32-i) programmable by said column signals to generate one of two signals having different logic levels, said spare signal generating circuits (32-1 to 32-i) being respectively coupled at the output terminals with first input terminals of said logic circuits (38-1 to 38-i), and an address designating circuit (34) programmable to have a specific address designating a defective bit-memory section, said address designating circuit (34) having an output terminal connected to second input terminals of said logic circuits (38-1 to 38-i), so that said one address designating circuit (34) can only contribute to the replacement of the defective memory column."

II. The reason given for the refusal was that the subject-matter of Claim 1 lacked an inventive step having regard to the prior art known from the following document:

D1: IBM Journal of Research and Development, vol. 24,
No. 3, May 1980, pages 291 to 298.

In the decision, it was said that the features of the precharacterising part of Claim 1 were clearly disclosed by the arrangement shown in Figure 8 in D1. The Examining Division had indicated in pencil, in an annex to the decision in the said Figure 8 of D1, which parts of the said arrangement corresponded to the features of Claim 1. In the said Figure 8, "data latch #1" and "data latch #2" together were considered as corresponding to "further switching means" according to Claim 1 and "redundant data latch #1" and "redundant data latch #2" were considered to correspond to the said "switching means" in Claim 1.

It was also said in the impugned decision that the features of the first two paragraphs of the characterising part of Claim 1 "are directly readable from Figure 8 of D1 because the bit switches and the redundant bit switches are only necessary to electrically separate the respective memory sections from the switching means and the further switching means, and can be neglected for functional considerations such that the switching means and the further switching means are directly coupled to the spare bit-memory sections and the bit-memory sections respectively".

It was moreover said that in the third paragraph of the characterising part of Claim 1 the control means (16-1, 16-2) were identified in that the features

- a plurality of logic circuits (38-1 to 38-i) and
- a plurality of spare signal generating circuits (32-1 to 32-i)

were specified in a detailed way and that they could not be directly identified in Figure 8 of D1. However, having regard to the functions of the arrangement of Figure 8, it was obvious to a skilled man to use the circuits identified in Claim 1 for implementing the said functions.

III. On 3 June 1992 the Appellant filed a notice of appeal against the decision and paid the appeal fee on the same day. The Statement of Grounds was filed on 3 August 1992.

IV. According to his main request, the Appellant requested that the decision under Appeal be set aside and a patent granted on the basis of the following documents:

- Claims 1 to 6 filed on 10 October 1991,
- description pages 1 to 3 and 6 to 12 as originally filed,
- description pages 4, 5 and 13 filed on 7 June 1988,
- description page 4a filed on 16 May 1989 and
- drawing sheets 1/7 to 5/7 including Figures 1 to 6 as originally filed.

The Appellant also requested oral proceedings in the case the Board of Appeal intended to confirm the impugned decision.

The Appellant moreover under an auxiliary request filed a new set of Claims 1 to 5.

V. The Appellant's arguments submitted in support of his requests can be summarised as follows:

In the semiconductor memory device according to the invention, "inhibit read strobe circuitry", "data latches #1, #2" and "redundant data latches #1, #2" (which all are necessary in the memory device of D1), are not required. "In the semiconductor memory device of document D1, data latches #1, #2 and redundant data latches #1, #2 operate to hold for a predetermined time the data which are supplied from bit switches and redundant bit lines #1, #2 respectively and decrease the capacitance. They do not operate as the switching means of the present invention." In the memory device according to D1 there is no switching means which is coupled with the spare bit-memory, further switching means which disconnects one or more defective bit-memory sections, and control means which turns on the switching means and at the same time turns off the further switching means when failure occurs in the memory cells. With the claimed design the memory device according to the invention can compensate for the defective bit-memory sections very quickly. Moreover, it is now clearly expressed in Claim 1 how said spare signal generating circuits and said address designating circuit of the control means are designed and how they cooperate in order to perform the said switch off/switch on operation when a defective bit-memory section is addressed.

Reasons for the Decision

1. The appeal is admissible.

Main request

2. D1 is the only document mentioned in the impugned decision. Figure 8 in this document discloses a block diagram for a two-bit chip containing two "output pads" ("data pad #1" and "data pad #2") each gated into 16 bit

lines through "data latches" ("data latch #1" and "data latch #2"). To these bit lines two redundant bit lines are added, which are connected over additional (unique) "redundant data latches" ("redundant data latch #1" and "redundant data latch #2") and "data pass devices" to the said "data output pads". The redundant bit lines and the bit lines are connected to the said "redundant data latches" and to the said "data latches" over "redundant bit switches" and "bit switches" respectively. Both the "data latches" and the "redundant data latches" are controlled by a read strobe from an "inhibit read strobe circuitry". Thus a defective bit line is isolated by inhibiting the "data latch" associated with this replaced bit line. The redundant line is then steered to the particular data path over the said "data pass devices" by a "bit steering and enable" circuit. Moreover the arrangement in Figure 8 contains an address designating circuit ("compare circuitry"), which - when a corresponding address is received - turns on a "redundant bit switch" of a corresponding redundant bit line connected to a corresponding "redundant data latch" and also activates said "inhibit read circuitry".

The Board is of the opinion that Claim 1 has been correctly delimited against the arrangement disclosed in D1 and that the characterising features of Claim 1 cannot be read onto Figure 8 in D1. The Board thus agrees with the opinion expressed by the Examining Division in a consultation by telephone on 11 September 1990, wherein in fact the composition of the present Claim 1 was suggested. In the minutes of said consultation the said "data pass devices" in D1 are considered by the Examining Division as corresponding to the said "switching means" of Claim 1.

The subject-matter of Claim 1 is therefore novel.

3. Thus the Board does not share the opinion of the Examining Division as expressed in the impugned decision, that the first two paragraphs of the characterising part of Claim 1 are directly readable onto Figure 8 of D1. Although the memory device shown in Figure 8 functions in a similar way as the device according to the invention, it is nevertheless different and, in particular, works in a different way. It does not appear to be correct to consider the said latches as the said switching means. A latch could under certain circumstances work similarly to a switch, but it is principally a memory element and in the present case, it seems that the said latches could not be comparable to the said switches according to the invention.

It is also noted that in the course of the proceedings the Examining Division has changed its mind concerning the said switching means several times. In the second communication, the said "bit switches" of the redundant bit lines and of the bit lines of D1 were considered to correspond to said switching and said further switching means of the present invention respectively; in the third and in the fourth communication the said "redundant data latches" and the said "data latches" of D1 were considered as such means.

As pointed out above, in the said telephone consultation (between the third and the fourth communications) the said "data pass devices" were seen as the said switching means.

All this appears to indicate that it is not that self-evident to arrive at the interpretation of D1 as suggested by the Examining Division in the impugned decision. It rather appears that this interpretation can only be made on the basis of an ex post facto analysis. It seems to the

Board that - when starting from the memory device disclosed in Figure 8 in D1 -the skilled man would not arrive at this interpretation without knowing the present application and he may not be expected to realise that the said latches could be considered as said switching means or realise that said latches could be replaced by such switching means. It, therefore, appears that already such an interpretation would contribute to an inventive step underlying the device according to Claim 1.

The Examining Division suggested that the features of the last paragraph of Claim 1, which principally correspond to the features of original Claim 2, should be introduced into Claim 1 in the course of the telephone consultation mentioned above. It was said that there were no indications in D1 how the control means could be realised. The Board fully agrees with that and cannot see how all these features which in fact identify an important part of the control system of the claimed memory device could be obvious to a skilled man having regard to the prior art disclosed in D1. This document does not disclose any of these features, which is understandable as D1 discloses an arrangement which for its proper functioning uses latches (and not switches), which are controlled by a control system (inhibit read strobe circuitry), the design of which is not disclosed in D1.

The present application as well as the cited document D1 are concerned with the general problem of providing memory devices which can compensate for defective memory cells using a small number of spare memory cells. However, the ways in which they propose to solve this problem are different.

Although the characterising features of Claim 1 may seem trivial, there is no hint in the state of the art towards

the solution according to the invention. This solution, however, is straight-forward and simple and avoids the use of data latches and redundant data latches which are necessary in the prior art device.

In the result, the Board therefore takes the view that the memory device according to Claim 1 involves an inventive step (Article 56 EPC) over the cited prior art.

Auxiliary requests

- 4. Since the main request of the Appellant is allowable, neither oral proceedings nor an examination of the auxiliary request are necessary.

Order

For these reasons, it is decided that:

- 1. The decision under appeal is set aside.
- 2. The case is remitted to the Examining Division with the order to grant a patent on the basis of the Appellant's main request (cf. under IV above).

The Registrar:



M. Kiehl

The Chairman:



P.K.J. van den Berg

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