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D E C I S I O N
of 28 July 1994

Case Number: T 0798/92 - 3.4.1

Application Number: 89200134.8

Publication Number: 0326218

IPC: H01L 21/90

Language of the proceedings: EN

Title of invention:
Method of manufacturing a semiconductor device, in which a metal conductor track is provided on a surface of a semiconductor body

Applicant:
N.V. Philips' Gloeilampenfabrieken

Opponent:
-

Headword:
-

Relevant legal norms:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
T 0109/82; T 0002/83; T 0225/84

Catchword:
-

Case Number: T 0798/92 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 28 July 1994

Appellant: N.V. Philip's Gloeilampenfabrieken
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 6 April 1992 refusing European patent application No. 89 200 134.8 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. D. Paterson
Members: Y. J. F. van Henden
J. H. Reich

Summary of Facts and Submissions

I. This European patent application was refused by decision of the Examining Division.

Claim 1 of this application reads

"A method of manufacturing a semiconductor device comprising a semiconductor body having a surface adjoined by a semiconductor region and a field oxide region surrounding said region, this surface being provided with a metal layer, in which a conductor track is formed, after which an isolating layer of silicon oxide is deposited over the semiconductor track on the surface, characterised in that, before the layer of silicon oxide is provided over the conductor track, this track is provided with a top layer of an oxidation-preventing material".

To this claim are appended further claims numbered 2 to 9.

II. The reason given for the refusal was that, having regard to the state of the art disclosed in, inter alia, documents

D1: EP-A-0 190 070 and
D3: Hsun-Hua Tseng el al. "a new Oxidation-Resistant Self-aligned $TiSi_2$ Process", in IEEE Electron Device Letters, Vol. EDL-7, No. 11 (November 1986), pages 623 to 624,

the subject-matter of Claim 1 lacked an inventive step.

III. The applicant lodged an appeal against the decision of the Examining Division.

IV. In a communication pursuant to Article 11(2) RPBA, the Board cited, as well as (D1) and (D3), the further documents

D4: R.A.M. Wolters et al. "Properties of Reactive Sputtered TiW", in "Solid State Technology", Vol. 29, No. 2 (February 1986), pages 131 to 136, and

D5: DE-A-3 414 781,

and expressed the provisory view that, having regard to the state of the art disclosed in these documents and having regard also to decision T 109/82 (OJ EPO 1984, 473), no claim of the patent application in suit seemed to involve an inventive step. The Board further explained why, in Claim 1, the designation "semiconductor track" had probably to be replaced by "conductor track".

V. Oral proceedings were held on 28 July 1994.

During the oral proceedings, the Appellant agreed to the replacement of "semiconductor track" by "conductor track" in Claim 1 and requested that a patent be granted on the basis of such an amended claim.

VI. In support of its request, the Appellant argued substantially as follows:

Document (D3) describes a SALICIDE process which is very similar to the subject-matter of the present application, and it also reveals that a superficial portion of a metal layer can be oxidised when exposed to air or oxygen. It furthermore discloses that, owing to the high reactivity of Ti with N_2, O_2 and H_2O, titanium losses cannot be completely prevented, especially when the initial thickness of the Ti film is very small. As already explained, however, the oxidised surface portion would not be such as to lead to the problems which the invention has for its object to solve.

A skilled person having read (D1) would understand that, while the silicon dioxide layer (42) is being formed by low pressure chemical vapour deposition, the metal tracks (30,B) are exposed to oxygen. Nevertheless, he would expect that, as soon as a thin silicon oxide layer has been formed, the underlying metal is shielded from oxidation, with the consequence that the very thin layer of metal oxide formed in the meantime would not substantially affect the resistance of the track, and even less result in an interruption of the latter. Therefore, it is not obvious to an average practitioner to adopt the measures known from (D3) while carrying out the method of (D1).

The inventors, however, found that a metallic conductor track formed on a semiconductor body and on which a layer of silicon oxide is subsequently deposited may have a much larger electrical resistance than could be expected. In certain cases, it has even been found that the conductor track is entirely interrupted. Therefore, the subject-matter of Claim 1 involves an inventive step.

During the oral proceedings of 28 July 1994, the Appellant submitted that, in normal use, one would just find out that a semiconductor device comprising defective conductor tracks does not function as it should do. The shortcomings mentioned in the paragraph bridging columns 1 and 2 of the published patent application would, however, not come to light, so that Decision T 109/82 is not relevant to the present case. Besides, the electrical resistance cannot be measured before completion of the interconnecting structure, i.e. before having carried out the following steps:

1) deposition of a layer of the metal;
2) forming a first photoresist mask;
3) forming the conductor tracks in the metal layer by etching;
4) removing the first photoresist mask;
5) deposition of a layer of silicon oxide;
6) forming a second photoresist mask;
7) forming contact windows in the silicon oxide by etching;
8) removing the second photoresist mask;
9) deposition of a layer of aluminium;
10) forming a third photoresist mask;
11) forming contacts to the conductor tracks by etching and
12) removing the third photoresist mask.

Since each of these steps can influence the resistance of the conductor tracks, inventiveness was required to identify the crucial one. Likewise, there is no ground to assert that a skilled person would perform a chemical analysis to find out why a conductor track is interrupted, nor that he would find that the failure originates in the oxidation of the latter. Finally, document (D4) does not show that most of the layer of TiW present in the contact window of Figure 10 or at the edges of said window would be oxidised.

VII. At the end of the oral proceedings, the decision was announced that the appeal is dismissed.

Reasons for the Decision

1. In the preamble to the description of the patent application, it is acknowledged that document (D1) discloses a method of manufacturing a semiconductor device such as defined by the pre-characterising part of Claim 1. The only matter at issue is that of inventive step.

2. Like most industrial products, integrated circuits are submitted to quality controls and, for this purpose, undergo technical tests, sometimes immediately after selected critical steps of the manufacturing process have been carried out. Such is in particular the case when perfecting the design of these circuits previous to starting their mass production. Therefore, even if it is accepted that the electrical resistance of conductor tracks provided in a semiconductor device can only be measured after completion of the interconnecting structure, it is nevertheless clear that the presence of conductor tracks having a much higher electrical resistance than was expected belongs to the category of deficiencies in an object which come to light when said object is tested prior to use.

As stated in paragraph VI above, the Appellant has submitted that Decision T 109/82 was not relevant to the present case, because it is concerned with a case where the posing of a new problem in connection with a known device was not considered to contribute to an inventive step because the deficiency in the known device which was underlying the new problem would have come to light when the device was in use.

According to the case law of the Boards of Appeal, it is well established that in principle, the posing of a new problem can contribute to the inventive step underlying a claimed invention - see for example Decisions T 2/83 (OJ EPO 1984, 265) and T 225/84 (EPOR 1986, 263). However, it was held in Decision T 109/82 that the "posing of a new problem does not represent a contribution to the inventive merits of the solution if it could have been posed by the average person skilled in the art". The present Board agrees with this finding. The case with which that decision was concerned, where the problem would have come to light when the known device was in use, is but one example where the problem could have been posed by the average skilled person.

The first question to be considered in the present case is therefore whether or not the skilled person would have perceived and posed the problem underlying the present claimed invention, namely that the resistance of the conductor track is too high as a result of the deposition of a layer of silicon oxide upon it.

3. When assessing inventive step in the case of semiconductor devices, it must be borne in mind that

the relevant skilled person is an engineer or a physicist having received a scientific education of university level. When observing that the electrical resistance of a conductor track formed on a semiconductor body is much higher than was expected, or even that the track is entirely interrupted, said skilled person will investigate the possible causes of the defect. Doing this is indeed part of his routine work while perfecting the design of new integrated circuits. Furthermore, in order to circumscribe the field of his search, he will try to find when the drawback appears, i.e. to identify the particular step in the manufacturing process during which the electrical resistance of the conductor track increases.

The Appellant submitted that, after a semiconductor body has been provided with circuit components such as transistors, at least the twelve steps recited in section VI of the present decision have to be carried out before the electrical resistance of the conductor tracks can be measured, and that the observed rise in electrical resistance is liable to occur during each one of the manufacturing steps following the formation of the tracks.

In the Board's view, however, a skilled person seeking to identify the manufacturing step which causes the unwanted increase in resistance would be expected to read the relevant state of the art in his technical field. In the present case, he would read document (D4) and learn therefrom that mixtures of tungsten and titanium to which nitrogen is added, are suitable for making conductor tracks on semiconductor bodies; that such mixtures are thermodynamically and kinetically capable of reducing silicon dioxide; and that the reduction of silicon dioxide is important because it removes the nascent oxide existing on silicon in the contact areas - see the paragraph headed "Contact Resistance" and from page 132, line 23 of the left-hand column, to the end of the paragraph headed "TiW as a Barrier Material". It is, however, clear that nascent oxide is only present in tiny quantities on the surface of a silicon substrate used for making a semiconductor device, so that the reduction of said oxide cannot lead to a dramatic decrease of the section of a conductor track formed on the substrate and consisting of a mixture of tungsten and titanium to which nitrogen is added. Nevertheless, the skilled person will be aware of the fact that certain metal layers used for conductor tracks are oxidised by a neighbouring silicon dioxide layer, because they have a higher chemical affinity to oxygen than silicon. Furthermore, the Board cannot share the Appellant's view that the skilled person would expect the metal of the conductor tracks to be shielded from oxidation as soon as a thin silicon oxide layer is deposited upon it, and that only a negligible section of the conductor track would be transformed into oxide. It is indeed widely known that not all metal oxides protect the underlying metal against further oxidation. Therefore, a skilled person can reasonably be expected not to **rely** on the oxygen diffusion preventing effect of the growing silicon dioxide layer and on that of the nascent metal oxide on the surface of the conductor track, but to analyse the complete track section in view of the observable increase in resistivity. Likewise, the fact that, in relation to the window represented in Figure 10 of document (D4), the latter does not show any attack of the TiW layer including nitrogen is no evidence of such a shielding effect in view of the exclusively schematic nature of Figure 10. No indication regarding the thickness of the layers represented there can indeed be found in (D4). Besides, it is beyond doubt that, in the case of integrated circuits incorporating submicronic structures - see column 2 of the published patent application - any superficial oxidation of the conductor tracks would unacceptably affect the electrical resistance of said tracks.

In the Board's judgment, therefore, only elementary considerations are needed for the skilled person to understand that oxidation of the conductor tracks occurs during or immediately after the deposition of the layer of silicon oxide.

4. Moreover, especially when conductor tracks are interrupted, any rise in the electrical resistance of such tracks hints at a reduction of the conduction section, hence at a possible alteration of the material forming the tracks. Therefore, an incentive to perform a chemical analysis of the remaining material is anyway given to the skilled person, whereby the presence of oxide(s) of the constituent material(s) of the tracks will normally be detectable by conventional means and thus provide evidence that the observed increase in electrical resistance originates in the oxidation of the conductor tracks. At this stage - being aware of the origin and cause of the defect - no exercise of inventive ingenuity is required to coat the conductor tracks with a top layer of a material which protects them against oxidation during subsequent steps of the process of manufacturing semiconductor devices. For instance an oxidation preventing layer of amorphous

silicon with a thickness of at least 3 μm, which is applied in the preferred embodiment claimed in Claim 3 of the application, is disclosed in document (D3) for the identical purpose - see page 623, left-hand column, paragraph 2.

5. In the Board's judgment, therefore, Claim 1 according to the Appellant's single request lacks an inventive step.

Said claim, therefore, is not allowable - Article 52(1) EPC in conjunction with Article 56 EPC. The application has accordingly to be refused.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer G. D. Paterson