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D E C I S I O N
of 9 November 1994

Case Number: T 0976/92 - 3.5.2

Application Number: 84302477.9

Publication Number: 0125790

IPC: H03L 7/18

Language of the proceedings: EN

Title of invention:
Frequency synthesisers

Patentee:
MARCONI INSTRUMENTS LIMITED

Opponent:
RACAL RESEARCH LIMITED

Headword:

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - yes (after amendment)"

Decisions cited:

Catchword:

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Case Number: T 0976/92 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 9 November 1994

Appellant/Respondent: (Opponent)
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Decision under appeal: **Interlocutory decision of the Opposition Division of the European Patent Office dated 17 August 1992 concerning maintenance of European patent No. 0 125 790 in amended form.**

Composition of the Board:

Chairman: R. E. Persson
Members: L. Toernroth
W. J. L. Wheeler

Summary of Facts and Submissions

I. Both the Patentee and the Opponent lodged an appeal against the interlocutory decision of the Opposition Division on the amended form in which the European patent No. 0 125 790 can be maintained.

The opposition was filed against the patent as a whole and was based on Article 100(a), (b), (c) EPC.

The Opposition Division held that the grounds for opposition mentioned in Article 100 EPC did not prejudice the maintenance of the patent as amended, having regard, inter alia, to the following document:

D1: US-A-4 204 174.

II. In the oral proceedings which were held before the Board on 9 November 1994 the Patentee filed a new set of Claims 1 to 8.

Independent Claims 1 and 4 now on file read:

"1. A frequency synthesiser including a phase locked loop including a variable frequency oscillator (1), the output of which is fed via a frequency divider (5) having a variable integer divisor value to a phase comparator (7), where it is compared with a reference frequency, the phase comparator being arranged to generate a control signal which is dependent on said comparison and which is fed via a low pass loop filter to control the frequency of said oscillator; digital means (10, 11, 14) responsive to a fractional divisor value for periodically altering the divisor value by a predetermined integer amount so that the effective divisor simulates said fractional divisor value;

characterised by said digital means (10, 14, 15, 16, 17) including phase correction means for progressively offsetting phase differences present at said phase comparator which stem from the alteration of the divisor value by said predetermined integer amount, said phase correction means being arranged to make periodic alterations to the divisor value additional to those made so that the effective divisor simulates said fractional divisor value, said additional alterations being in accordance with a plurality of predetermined sequences which represent successive rows of Pascal's triangle, the terms of which all sum to zero, said phase correction means comprising a plurality of successive stages, each of which alters said divisor value in accordance with a respective one of said predetermined sequences, said successive stages progressively reducing the low frequency content of the waveform comprising said phase comparator phase differences so that when said control signal generated by said phase comparator is fed via said low pass loop filter the resultant phase noise present in the output frequencies generated by said synthesiser is reduced."

"4. A frequency synthesiser including a phase locked loop including a variable frequency oscillator (1), the output of which is fed via a frequency divider (5) having a variable integer divisor value to a phase comparator (7), where it is compared with a reference frequency, the phase comparator being arranged to generate a control signal which is dependent on said comparison and which is fed via a low pass loop filter to control the frequency of said oscillator, first clocked accumulator means (14) responsive to a fractional divisor value for periodically altering the divisor value by a predetermined integer amount when its contents reaches or exceeds a predetermined value so that the effective divisor simulates said fractional

divisor value; characterised by digital phase correction means for progressively offsetting phase differences at said phase comparator which stem from the alteration of the divisor value by said predetermined integer amount, said phase correction means comprising a cascaded plurality of further clocked accumulator means (15, 16, 17) each of which is arranged to periodically alter the divisor value in accordance with a respective predetermined sequence, the terms of which all sum to zero, each accumulator means being arranged to integrate the contents of the preceding accumulator means, each said further accumulator means (15 or 16 or 17) comprising a stage of said digital phase correction means, said plurality of further accumulator means (15, 16, 17) together comprising a plurality of successive stages of said digital phase correction means, said successive stages progressively reducing the low frequency content of the waveform comprising said phase comparator phase differences so that when said control signal generated by said phase comparator is fed via said low pass loop filter the resultant phase noise present in the output frequencies generated by said synthesiser is reduced."

Claims 2 and 3, and Claims 5 to 8 are dependent on Claims 1 and 4 respectively.

III. The Patentee requested that the patent be maintained on the basis of Claims 1 to 8 as submitted in the oral proceedings, and argued essentially as follows:

According to the contested patent, undesirable phase modulation in a PLL-frequency synthesiser responsive to fractional divisor values was progressively reduced in the loop filter's pass band by means of a plurality of successive stages of correction which shifted the frequency spectrum of the phase noise to higher

frequencies by making integer alterations to the divisor value in accordance with predetermined sequences, whose terms summed to zero. Claim 1 defined these sequences as the rows of Pascal's triangle. On the basis of this teaching and with the help of computer simulation, the person skilled in the art would be able to find other sequences providing satisfactory phase correction. Claim 4 was meant to cover such alternative sequences and, therefore, found sufficient support in the teaching of the contested patent.

In the frequency synthesiser known from D1 (fig. 1), a first accumulator 78 was responsible for generating a fractional divisor value, whereas a second accumulator 90 and an associated differentiating circuit made additional adjustments to the divisor value in order to reduce the phase error at the phase comparator's output to a level at which it could be corrected across the whole frequency spectrum by an analog circuit (34, 104, 108) made from low tolerance components. D1, however, did not hint at the possibility of using a plurality of digital stages to perform digital integrations and differentiations of increasing order for the purpose of phase correction. Therefore, it would not have been obvious to the skilled person starting from D1 to add a further accumulator in cascade with the accumulator 90 and a digital differentiating circuit for performing second order differentiation of the carry signals from said further accumulator. The subject-matter of both Claims 1 and 4 involved an inventive step within the meaning of Article 56 EPC.

IV. The Opponent requested that the decision under appeal be set aside and the patent revoked, and argued essentially as follows:

The only embodiment clearly disclosed in the contested patent (fig. 1) and the frequency synthesiser according to the closest prior art document D1 (fig. 3) showed similarities which were not accidental. Both had a first accumulator (14, fig. 1 of the patent; 78, fig. 3 of D1), which produced periodical integer changes of the divisor, and a second accumulator (15, fig. 1 of the patent; 90, fig. 3 of D1) with a delay stage which altered the divisor value according to a predetermined sequence (+1, -1) corresponding to the second row of Pascal's triangle. It was clear from D1 that the accumulator 90 integrated the output from the accumulator 78 (D1, column 6, lines 45 to 46) and that the corresponding delay line differentiated the carry over pulses from said accumulator (column 7, lines 19 to 21) to perform consecutive adjustments of the phase differences by means of temporary repetitive phase shifts (D1, column 9, lines 56 to 60). The addition of further temporary repetitive phase shifts in the arrangement shown in D1 was a straightforward improvement which involved at least the integration of the output from the accumulator 90 and the second order differentiation of the corresponding carry over pulses. As it was commonly known, the coefficients needed in multiple digital differentiations were the terms of the rows of Pascal's triangle. Hence, it would have been obvious to the person skilled in the art to add at least one further clocked accumulator and differentiation stage to the frequency synthesiser disclosed in D1 and thus arrive at an arrangement falling within the terms of Claims 1 and 4. Therefore, the subject-matter of the independent claims did not involve an inventive step within the meaning of Article 56 EPC. Furthermore, Claim 4 was based on some general statements about the sequences. These statements, however, corresponded to some general comments made in the patent, which were directed to the terms of Pascal's triangle. The

specification did not indicate what sequences were useful and gave no guidance as to how sequences other than the terms of Pascal's triangle could be determined. Therefore, the subject-matter of Claim 4 had no support.

Reasons for the Decision

1. The appeals are admissible.

2. The Board considers that the new independent Claims 1 and 4 filed in the oral proceedings comply with Article 123(2) and (3) EPC and that their subject-matter is novel within the meaning of Article 54 EPC.

3.1 Document D1 is regarded as the closest prior art. It discloses a frequency synthesiser comprising the following features recited in the preambles of Claims 1 and 4:

- a phase locked loop including a variable frequency oscillator 10, the output of which is fed via a frequency divider 14 having a variable integer divisor value to a phase comparator 18, where it is compared with a reference frequency, the phase comparator being arranged to generate a control signal which is dependent on said comparison and which is fed via a low pass loop filter 23 to control the frequency of said oscillator,

- digital means in the form of first clocked accumulator means 78 responsive to a fractional divisor value for periodically altering the divisor value by a predetermined integer amount (one) when

its contents reaches or exceeds a predetermined value so that the effective divisor simulates said fractional divisor value.

3.2 The frequency synthesiser according to D1 further has phase correction means for offsetting phase differences at the phase comparator 18 which stem from the alteration of the divisor value by said predetermined integer amount. Said phase correction means comprises:

- a clocked accumulator 90 arranged to integrate the contents of the preceding accumulator 78 and to alter the divisor value periodically in accordance with a predetermined sequence (+1, -1), whose terms sum to zero and represent a row of Pascal's triangle (but this is not mentioned in D1), and

- an analog circuit (34, 104, 108) producing a phase correction signal from the output of the second accumulator means 90.

3.3 The subject-matter of Claim 1 and Claim 4 differs from the frequency synthesiser shown in D1 essentially in that the phase correction means, comprises a **plurality** of successive digital stages (15, 16, 17, ...), each of which alters the divisor value in accordance with a respective one of a **plurality** of predetermined sequences. These sequences are specified in Claim 1 as successive rows of **Pascal's triangle**, whereas in Claim 4 they are defined as having terms which add to zero.

3.4 According to the Opponent, the question which needs to be addressed in the present appeal is whether it would be obvious to the skilled person to add at least a further clocked accumulator and a corresponding differentiation stage to the arrangement described in

D1, since such an addition would indeed result in a frequency synthesiser falling within the terms of Claims 1 and 4.

3.5 It is stated in D1 that the accumulator 90 integrates the output signal from the accumulator 78 (column 6, lines 45 to 48) and that the delay line 98 and the adder 80 act to differentiate the carry over signals from the accumulator 90 which represent the integral of phase (column 7, lines 19 to 21). This first order digital differentiation is performed by altering the divisor value according to a sequence (+1, -1). Although, with the benefit of hindsight, it can be seen that the terms of this sequence correspond to the second row of Pascal's triangle, this fact is not mentioned in D1.

3.6 The Opponent argued that, since the function performed by the accumulator 90 and its associated delay 98 is to produce semi-continuous adjustments to the phase difference at the phase comparator's output (cf. D1, column 9, lines 56 to 60), it would be obvious to improve the performance of the prior art frequency synthesiser simply by adding further temporary repetitive shifts of the phase. This would imply the addition of at least a further accumulator integrating the output from the accumulator 90 and an associated delay circuit to perform second order differentiation, i.e. to alter the divisor in accordance with a sequence corresponding to the third row of Pascal's triangle (+1, -2, +1).

3.7 In D1, however, there is no hint that additional temporary phase shifts before the analog phase correction could have any advantageous effect on the phase correction or that successive stages performing higher order integrations and differentiations could altogether replace the analog phase compensation

circuit. Actually, D1 teaches to reduce phase noise in two stages: first, additional instantaneous adjustments to the divisor are made between the step changes simulating the fractional value in order to limit the amplitude of the sawtooth waveform of the phase difference and change its wave shape; and, second, an analog signal is generated to back off the residual modulation (D1, column 4, lines 18 to 30).

3.8 In the frequency synthesiser according to the invention, the successive integration/differentiation stages do not aim at further reducing the phase differences at the output of the phase comparator. On the contrary, as pointed out by the Patentee, phase noise in total is increased, the gist of the invention consisting in moving the frequency spectrum of the phase noise to a range above the loop filter's pass band. Furthermore, the addition of further integration and differentiation stages to the arrangement shown in D1 would not be in conformity with the teaching of D1, which specifies that the result of the digital correction stage is simply to convert the sawtooth waveform to a much smaller or residual waveform which varies around zero (column 8, lines 23 to 26), which can be backed off "by means of an analog output which does not have to be produced by close tolerance components" (cf. D1, column 1, lines 64 to 68) and that additional smoothing of the phase difference in the control loop is avoided (D1, column 4, lines 26 to 30).

3.9 In the result, the Board finds that, in the light of the prior art teaching and the general knowledge in the art, it would not be obvious to the skilled person starting from D1 to arrive at a frequency synthesiser falling within the terms of Claim 1 or Claim 4. Thus, the subject-matter of these claims involves an inventive step within the meaning of Article 56 EPC.

4.1 The Opponent objected that the definition of the sequences provided in Claim 4 relied only on some general statements which in the patent specification were only related to the terms of Pascal's triangle and that, therefore, the patent did not give any guidance as to how other useful sequences could be determined.

4.2 The functional features recited in the Claim 4 make clear that this independent claim is not meant to cover all possible sequences whose terms add to zero, but that it is only directed to those sequences which are suitable for reducing the low frequency content of the phase noise. The Board agrees with the Patentee that the skilled person reading the patent specification would realize that the benefits of the invention may probably be obtainable with other sequences than those corresponding to the terms of Pascal's triangle, though the latter may provide the best result, and that it would be straightforward for the skilled person to discover such sequences with the help of computer simulation. Hence, the Board considers that the subject-matter of Claim 4 has sufficient support in the teaching of the patent in suit.

5. For the above reasons, the Board finds that Claims 1 and 4 meet the requirements of the EPC. Consequently, a patent can be maintained on the basis of these claims. The same applies to the dependent Claims 2, 3 and 5 to 8. The description and the drawings do not appear to require any adaptation.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The patent is to be maintained on the basis of Claims 1 to 8 as submitted in the oral proceedings.

The Registrar: The Chairman:

M. Krehl E. Persson