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D E C I S I O N
of 9 August 1995

Case Number: T 0979/92 - 3.4.1

Application Number: 88201774.2

Publication Number: 0305001

IPC: H01L 23/52

Language of the proceedings: EN

Title of invention:
Integrated semiconductor circuit with decoupled D.C. wiring

Applicant:
Philips Electronics N.V.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"
"Analogous use of a known measure"

Decisions cited:
-

Catchword:
-

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Case Number: T 0979/92 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 9 August 1995

Appellant: Philips Electronics N.V.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 11 June 1992 refusing European patent application No. 88 201 774.2 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. D. Paterson
Members: H. J. Reich
R. K. Shukla

Summary of Facts and Submissions

I. European patent application No. 88 201 774.2 (publication No. 0 305 001) was refused by a decision of the Examining Division.

Claim 1 as originally filed reads as follows:

"1. An integrated semiconductor circuit comprising a semiconductor region adjoining a surface of a semiconductor body and covered with an electrically insulating layer, the semiconductor region including a plurality of semiconductor circuit elements interconnected by conductor tracks disposed on the insulating layer and constituting the wiring of the circuit, a part of the wiring being only intended to contain D.C. information and constituting the D.C. wiring, characterized in that the insulating layer under at least a substantial part of the D.C. wiring is considerably thinner than under the wiring parts not forming part of the D.C. wiring, this thinner part being located on a part of the semiconductor surface which is connected to a connection conductor."

Claims 2 to 7 are dependent on Claim 1.

II. The reason given for the refusal was that the subject-matter of Claim 1 as originally filed lacked novelty for the Contracting States DE, FR and GB pursuant to Articles 54(3) and (4) EPC in view of the disclosure in document

D3: EP-A-0 263 289,

and moreover did not satisfy the requirements of Articles 52 and 56 EPC having regard to documents:

D2: GB-A-2 087 183, and
D1: US-A-4 190 854

for the following reasons: Document D2 discloses, in particular in Figures 9, 10 and 12 to 14, integration of capacitive structures into the D.C. wiring of an integrated circuit in order to decouple it from high frequency interferences. Wirings 17 in Figure 9; 171, 172 in Figure 10 and RL-line in Figures 13 and 14 carry D.C. voltages and are part of the interconnection wiring of the integrated circuit. The possibility to increase capacitance, not by an increase of the capacitor area, but by decreasing the thickness of the insulating layer is shown by document D1 and even in Figure 10 of document D2. Although document D1 refers primarily to a trimmable capacitor structure integrated into the circuit wiring, it informs the skilled person about the possibility of forming required capacitive structures by integral parts of the wiring which are partially formed on thinned regions of the underlying insulating layer. The application of the teaching of document D2, i.e. to integrate decoupling capacitor structures directly into the D.C. wiring, in the circuit known from document D1 would lead the skilled person directly to the subject-matter of Claim 1.

III. The Appellant lodged an appeal against this decision, contesting inter alia the technical relevance of the disclosures in documents D1 and D3.

IV. In a communication accompanying a summons to oral proceedings, the Board expressed its preliminary view which can be summarised as follows: The closest prior art is represented by the embodiment disclosed in

Figures 6 and 10 of document D2. Document D2 is silent about the extension of parts of the D.C. wiring 171 and 172 shown in Figure 10, under which the insulating layer is considerably thinner.

Document

D4: EP-A-0 230 154

cited in the European Search Report, teaches on page 3, lines 10 to 14 and 19 to 21 in combination with the embodiment in Figure 17 and page 12, lines 12 to 25 to reduce induced HF noise in busses by providing capacitance means "along" and "beneath" the busses for "minimising impact on the space in the structure". In view of this known concept, it would appear to be obvious to extend the area of the thinned insulating layer regions 11' - together with channel layers 12' and 13' - so that they are "under at least a substantial part" of the D.C. wiring V_{REF} in Figures 6 and 10 of document D2 and thus to arrive at the subject-matter claimed in Claim 1.

V. Oral proceedings were held before the Board on 9 August 1995, at the end of which the Appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of Claim 1 as originally filed (main request), or as filed during the oral proceedings (auxiliary request).

In Claim 1 of the auxiliary request, the wording of Claim 1 of the main request; "... a substantial part of the D.C. wiring ..." is amended into "... a substantial part **of the length** of the D.C. wiring".

VI. In support of his requests the Appellant argued essentially as follows:

(a) Figures 6 and 10 of document D2 show **discrete** capacitors C_1 and C_2, the electrodes (171, 172; 12', 13') of which are electrically connected to wiring lines RL and PL and RL and GL respectively. Document D2 discloses with regard to the embodiment of Figure 4 on page 4, lines 25 to 32 that D.C. wiring line RL itself forms relatively small parasitic capacitors C11 and C21. This statement clearly shows that the conventional D.C. wiring itself is not provided on the thinner insulating layer and thereby not used as a part of a decoupling capacitor. Hence, document D2 teaches away from the solution claimed in the characterising part of Claim 1 which reduces noise and signal distortion in D.C. wirings induced by high-frequency interferences. According to this solution the thinned insulating layer underlying the D.c. wiring transforms the D.C. wiring itself into the upper electrode of the decoupling capacitance, requiring thus no additional chip area.

(b) In the invention the insulating layer under the A.C. wiring is kept sufficiently thick to avoid A.C information leaking away to the substrate. There is no indication in document D2 as to where and how wiring not forming part of the D.C. wiring is made.

(c) In the embodiment according to Figures 8 and 9 of document D2 the insulating layer 16 underlying aluminium layer 17 is nowhere thinned but its width is locally enlarged to form a decoupling capacitor

having a relatively large capacitance compared with the negligible parasitic capacitance in the wiring region.

(d) In the embodiment according to Figures 12 to 14 of document D2, the second capacitor electrode opposite the reference voltage wiring is not formed in the surface of the semiconductor substrate but by polycrystalline silicon layers 14 and 15 which are provided on an insulating film 11.

(e) With regard to the Board's interpretation of the disclosure in document D4 (see paragraph IV above), Figure 17 and page 12, lines 11 to 25 of document D4 disclose that metal layer 104 is used as an electrode layer of the capacitor. A skilled person will interpret the text, "Metal layer 104 **may also comprise** the V_{ss} bus or the V_{cc} bus" to mean that the same metal layer as is used for the capacitor electrode may also be used to make a bus line. There is no indication that the bus line is identical to the capacitor electrode for a substantial part of the D.C. wiring. Moreover, Figure 3A and page 6, line 4 to page 7, line 4 of document D4 clearly show that its general teaching "capacitance means ... distributed along the busses" means that **discrete** capacitors 16 are provided at several locations along the bus to compensate for the inductance in the lines.

(f) The wording of Claim 1 of the auxiliary request is intended to distinguish the invention more clearly from the embodiment in Figure 10 of document D2, which only shows a cross-section of the capacitor. No conclusion can be drawn therefrom about the structure of the capacitor over a substantial part of the length of the D.C. wiring.

VII. At the conclusion of the oral proceedings, the decision was announced that the appeal is dismissed.

Reasons for the Decision

1. In the Board's view, the wording of Claim 1 of the auxiliary request: "that the insulating layer under at least a substantial part **along the length** of the D.C. wiring is considerably thinner" merely clarifies the statement in Claim 1 of the main request, i.e. "that the insulating layer under at least a substantial part of the D.C. wiring is considerably thinner". The wording "along the length" is regarded to be implicit in the subject-matter of Claim 1 of the main request and is thus superfluous. Hence, Claims 1 of the main and auxiliary requests define identical subject-matter and can be dealt with together.

2. *Inventive step - Claims 1 - main and auxiliary requests*

2.1 From the closest prior art according to the embodiment in Figures 6 and 10 of document D2, there is known (in the wording of Claims 1 of the main and auxiliary requests):

"An integrated semiconductor circuit comprising a semiconductor region adjoining a surface of a semiconductor body and covered with an electrically insulating layer (see D2, 11 and 11' in Figure 10), the semiconductor region including a plurality of semiconductor circuit elements (4, VRG, AB and 3 in Figure 6) interconnected by conductor tracks (PL, GL and RL in Figure 6) disposed on the insulating layer (in analogy to tracks 171 and 172 in Figure 10) and constituting the wiring of the circuit, a part of the

wiring being only intended to contain D.C. information (RL) and constituting the D.C. wiring, characterized in that the insulating layer (11, 11' in Figure 10) under "the area of the upper electrode (171, 172 in Figure 10) of the decoupling capacitance (C_1, C_2 in Figure 6)" is considerably thinner (11') than under the wiring parts not forming part of the D.C. wiring (11), this thinner part (11') being located on a part of the semiconductor surface (12', 13') which is connected to a connection conductor (page 5, line 79 to 92)."

Document D2 gives no clear information whether tracks 171 and 172 in the embodiment according to Figure 10 only exercise the function of a filter decoupling HF noise or whether they are additionally used as interconnecting wiring for transmitting the D.C. reference potential (V_{REF}). Therefore, the Board regards the Appellant's submission in paragraph VI-(a) above to be plausible insofar as a cross-section of the semiconductor device according to Figure 10 represents only the area of the decoupling capacitances C_1 and C_2 and not the region of the interconnecting D.C. wiring V_{REF}. Also, contrary to the Appellant's argument in paragraph VI-(b) above, in the Board's view, having regard to the embodiment of Figure 4, page 4, lines 19 to 32, a skilled person is likely to interpret the schematic wiring between the terminal V_{REF} and the tracks 171 and 172 shown in Figure 10 as tracks provided on the thicker part (11) of the insulating layer in order to reduce parasitic capacitance of the interconnecting lines. The Board agrees with the Appellant's technical interpretation of the embodiment of Figures 8 and 9 of document D2 in paragraph VI-(c) above. However, in the assessment of inventive step, the embodiment in Figure 10 (thinner dielectric), and not that in Figure 8 (enlarged capacitor area), is regarded as the relevant technical starting point.

2.2 Starting from document D2, the objective problem underlying the invention as claimed in Claim 1 is - in line with the description of the present application, column 1, lines 12 to 31 and 41 to 48 - to provide a conventional decoupling capacitor for reducing noise and distortion in D.C. wiring parts in such a way that no additional semiconductor surface area is required. Increasing the integration density of circuits in integrated semiconductor circuits is a constant and known aim in the semiconductor device technology. Hence, no contribution to inventive step is to be found in the definition of the above problem.

Since an examination of Figures 8 and 10 of document D2 clearly demonstrates that for realising a given value of a decoupling capacitance either the upper electrode area is reduced or the capacitor dielectric is made thin, it would be obvious to the skilled person to select the concept of a thinned dielectric and to decide on Figure 10 as the technical starting point for his solution.

2.3 The above problem is solved in that the conventional area of the upper electrode (171, 172 in Figure 10) of the decoupling capacitance is replaced by "at least a substantial part (along the length) of the D.C. wiring". This solution implies the following technical modifications: If any enlarged track width would be realised in Figure 10, it has to be reduced to the track width of the V_{REF}-line. Furthermore, the conventional thinned insulating region 11' has to be extended under the V_{REF}-line until the upper electrode area (i.e. the area of the V_{REF}-line track), which is necessary for the desired value of the decoupling capacitance to be obtained. No additional technical measure is necessary in order to realise the claimed electric connection of the semiconductor surface under the thinned insulating

layer to a connection conductor, since reference potential V_{REF} automatically induces channel layer 12' in the semiconductor surface underlying the V_{REF}-line, see D2, page 5, lines 84 to 87.

2.4 In the Board's view the technical measures for realising the claimed solution as indicated above can be expected from a skilled person once he has found the concept underlying the claimed solution to use the D.C. wiring (i.e. in the case of document D2 the V_{REF}-line) additionally as the upper electrode of the decoupling capacitance; see also paragraph VI-(a) above. Hence, the examination of an inventive step underlying the subject-matter of Claims 1 of the main and auxiliary requests reduces to the question whether the state of the art hints a skilled person to the double function of a conductive track as interconnecting wiring and electrode of a HF-decoupling capacitor and thereby renders the claimed solution obvious.

2.5 Contrary to the Appellant's view in paragraph VI-(a) above, document D2 states (see embodiment in Figures 12 to 14) on page 6, lines 68 to 71 explicitly: "According to this embodiment, the reference voltage wiring RL formed in Sections A and B of Figure 12 constitutes the upper electrode of capacitor C_1 (Figure 13) and in Section B the upper electrode of capacitor C_2 (Figure 14)". The Board follows the view of the Examining Division in the decision under appeal (see paragraph II above) in that an integration of a capacitive structure into a D.C. wiring of an integrated circuit is known from the embodiment in Figures 12 to 14 of document D2. From Sections A and B of Figure 12 a skilled person clearly learns that via the double function of interconnecting wiring and of electrode no additional semiconductor surface area is required for a discrete decoupling capacitor. Hence, the outlay in

Figure 12 provides a hint to the concept of the claimed solution. Since the skilled person in the Board's view is able to verify that the advantage of saving semiconductor surface space by using an interconnecting wiring also as a first capacitor electrode, can be achieved independently of any particular requirement for the second capacitor electrode, the Appellant's argument according to paragraph VI-(d) above is not regarded as relevant.

2.6 Document D4 discloses on page 3, lines 10 to 14: "The reduction of induced voltage spikes is achieved by the provision of capacitance means distributed along the V_{cc} and V_{ss} busses, while minimising impact on the space in the structure". The Appellant's interpretation of this general teaching in the light of the embodiment of Figure 3A according to paragraph VI-(e) above, is regarded as only one of the possible alternatives disclosed in document D4. A limitation of the above wording to a sequence of discrete decoupling capacitors with upper electrode areas, which are intermittently provided along a bus is clearly contradictory to the teaching in document D4, page 3, lines 19 to 21: "In a preferred embodiment, the capacitance means comprises one or more capacitors formed **beneath** one or both of the busses". Although, the wording in document D4, page 12, lines 19 and 20: "Metal layer 104 (in Figure 17) may also comprise the V_{ss} bus or the V_{cc} bus" can be interpreted according to the submission of the Appellant in paragraph VI-(e) to mean that metal layer 104 may exclusively be a capacitor plate, in the Board's view this wording additionally implies that metal layer 104 in Figure 17 of document D4 carried out the double function of an interconnection wiring and a decoupling capacitor electrode. In combination with the above preferred embodiment of providing the decoupling capacitor **beneath** the busses, the skilled person would

consider the latter alternative to be a realistic approach and to derive from document D4 a hint to the concept underlying the claimed solution.

2.7 As set out in detail above, the subject-matter of Claims 1 of the main and auxiliary requests is the result of an analogous use of a known measure that an interconnecting D.C. wiring simultaneously constitutes the upper electrode of a HF decoupling capacitor - such as disclosed in document D4 or in Figures 12 to 14 of document D2 - in the (thinned dielectric) embodiment according to Figures 6 and 10 of document D2. Such a use of a known measure for exploiting its known effects must be regarded as obvious.

3. For the reasons set out above in paragraphs 2.1 and 2.7, Claims 1 of the main and auxiliary requests do not involve an inventive step and are not allowable pursuant to Articles 52(1) and (56) EPC. Claims 2 to 7 of both requests fall because of their dependence on the respective Claim 1.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer G. D. Paterson