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D E C I S I O N
of 22 August 1995

Case Number: T 0991/92 - 3.4.1

Application Number: 88104463.0

Publication Number: 0283991

IPC: H01L 21/28

Language of the proceedings: EN

Title of invention:
Method of manufacturing semiconductor device

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
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Case Number: T 0991/92 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 22 August 1995

Appellant:

KABUSHIKI KAISHA TOSHIBA
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi
Kanagawa-ken 210
Tokyo (JP)

Representative:

Polz, Leo
Hoffmann, Eitle & Partner
Patentanwälte
Postfach 81 04 20
D-81904 München (DE)

Decision under appeal:

Decision of the Examining Division of the European Patent Office dated 17 June 1992 refusing European patent application No. 88 104 463.0 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: G. D. Paterson
Members: H. J. Reich
U. G. O. Himmler

Summary of Facts and Submissions

I. European patent application No. 88 104 463.0 (publication No. 0 283 991) was refused by a decision of the Examining Division.

II. The reason given for the refusal was that the subject-matter of dependent Claim 9 filed on 16 March 1992 is not novel in view of document:

D1: EP-A-0 123 726

and does not meet the requirements of Article 52(1) and 54(1) and (2) EPC. The subject-matter according to Claim 1 as originally filed differs from that known from document D1 only in that the manufacturing steps claimed in Claim 9 have been omitted; i.e. that "said antioxidant film is removed from said second silicon layer before said conductive layer is formed on said silicon layer and said element isolation region". This omission is a normal design option for the skilled person, depending on if said conductive layer needs to be electrically connected to said second silicon layer. Therefore, the subject-matter of Claim 1 lacks an inventive step in the sense of Article 56 EPC. Furthermore, Claim 1 is not supported by the description since the description only discloses that said conductive layer is to be electrically connected to said second silicon layer which implies the removal of the antioxidant film prior to the deposition of said conductive layer.

III. The Appellant lodged an appeal against this decision. With its Statement of Grounds of Appeal the Appellant filed an amended Claim 1 which, in addition to the features of Claim 1 which was the subject of the decision under appeal, contained the following features:

(a) "said third insulating film (24) having such thickness as prevents a withstand voltage of said semiconductor device from decreasing"

(b) "said (conductive) layer (25) including a portion located on said second silicon layer (22)", and

(c) "a portion located on said element isolation region (18), and a portion in contact with said third insulating film (24)".

IV. In a communication accompanying a summons to oral proceedings, the Board informed the Appellant of its provisional view, that this amended Claim 1 is distinguished from the method disclosed in document D1 only by functional feature (a) mentioned above, which - with regard to the disclosure in D1, page 8, paragraph 2 and page 7, lines 17 to 21 - may be regarded as the result of a skilled person's routine dimensioning of the conventional side wall oxidation of first silicon layer 14" of document D1. In reply to this communication the Appellant filed on 27 July 1995 a further amended claim wherein the step of forming a first silicon layer (20) doped with an impurity was specified as: "forming a first silicon layer (20) doped with phosphorus in a high concentration".

V. Oral proceedings were held on 22 August 1995 during which the Appellant requested that the decision under appeal be set aside, and that a patent be granted on the basis of the main request filed during oral proceedings.

Claim 1 of this main request specified the high concentration of phosphorous to have the effect of increasing the speed of oxidation of the first silicon layer. Having regard to this newly added feature of increasing oxidation speed by phosphor doping, the Board drew the Appellant's attention to the disclosure in document D1, page 6, lines 10 to 13 with regard to the phosphor doping of the conventional first silicon layer 14 in combination with the oxidation thicknesses for layers 6' and 14" disclosed on page 8, paragraph 2. Furthermore, the Appellant was invited to comment on the oxidation mechanism of a silicon layer covered on both surfaces with SiO_2.

VI. Claim 1 of the main request handed over during the oral proceedings reads as follows:

"A method of manufacturing a semiconductor device, using two or more silicon layers, comprising the steps of:

(a) forming an element isolation region (18) on a major surface of a silicon substrate (17);

(b) forming a first insulating film (19) on an element region of said silicon substrate (17) which is isolated by said element isolation region (18);

(c) forming a first silicon layer (20) doped with phosphorus in a high concentration on said first insulating film (19) and said element isolation region (18);

(d) forming a second insulating film (21) on said first silicon layer (20);

(e) forming a second silicon layer (22) on said second insulating film (21);

(f) forming an antioxidant film (23) on said second silicon layer (22),

(g) selectively etching said antioxidant film (23), said second silicon layer (22), said second insulating

film (21), and said first silicon film (20) using a mask having a predetermined pattern;
(h) forming a third insulating film (24) on said wall portions of said first and second silicon layers (20, 22), by selective oxidation, using said antioxidant film as a mask, wherein said high concentration of phosphorus is contained in said first silicon layer (20) for increasing the speed of oxidation of said silicon layer (20) in step (h) to form said third insulating film (24) having such a thickness as prevents a withstand voltage of said semiconductor device from decreasing;
(i) forming a conductive layer (25) on said second silicon layer (22) and said element isolation region (18), said layer (25) including a portion located on said second silicon layer (22), a portion located on said element isolation region (18), and a portion in contact with said third insulating film (24)."

Claims 2 to 9 are dependent on claim 1.

VII. In support of this request the Appellant argued essentially as follows:

(a) The alternative with aligned first and second silicon layers (14" and 22") and second insulating film (16', 18', 20') formed in one etch step is only mentioned in one line of document D1; i.e. page 7, lines 17 to 21. A skilled person would not make use of this alternative when improving the time constancy of the withstand voltage, since an oxidation of such aligned structure does not allow to round the edges of the remaining first silicon layer and thus to avoid field enhancement. The skilled person would rely on the alternative disclosed in Figures 4 to 6 of document D1 with an extended region of the first silicon layer 14". In this alternative the edges of the first silicon

layer are surrounded by the oxidising gas atmosphere, so that the edge can be oxidised from all sides into a rounded form. Providing this rounding effect in an aligned structure (as disclosed in the present application Figure 3D and column 4, paragraph 2 of the description) by doping first silicon layer 20 with a high concentration of phosphorous is not obvious to a skilled person.

(b) The doping of first silicon layer (20) with phosphor in high concentration represents the essential feature of the present invention and is not obvious in view of the teaching of document D1. The doping mentioned in document D1, page 6, lines 10 to 13 relates to normal conductivity doping from which a skilled person would not derive "high concentration" doping as a means to increase the oxidation speed. The disclosure on page 8, paragraph 2 of document D1 relates the "faster rate" of the oxidation of first silicon layer 14" to that of the growth of the field oxide in region 4 and thus does not allow to conclude that the faster rate of oxidation is caused by phosphor doping. Whereas the method of document D1 realises sufficient insulation via a corresponding oxidation time, the invention makes use of a different and non-obvious solution, i.e. by increasing the conventional concentration of phosphor in the first silicon layer.

(c) Hence, a skilled reader will interpret the disclosure in the description of the present application, column 4, paragraph 2 reading "layer 20 contains a high concentration of phosphorus" in the sense of a concentration which is higher than

traditional values. The explicit disclosure in the description column 3, lines 43 to 47 reading "a concentration of about 2 x 10^{20} cm^{-3} is erroneous and should read: a concentration **higher** than 2 x 10^{20} cm^{-3}.

VIII. At the conclusion of the oral proceedings the decision was announced that the appeal was dismissed.

Reasons for the Decision

1. *Inventive step - Claim 1*

1.1 The alternative with aligned first and second silicon layers (14" and 22") and second insulating film (16', 18', 20') as disclosed in document D1, Figure 3 in combination with page 7, lines 17 to 21, is easily realisable by continuing the etch steps disclosed in Figure 3 to comprise the etching of first silicon layer 14 with the identically patterned mask. It is thus by no means a desideratum. Though only disclosed in Figure 3 and page 7, paragraph 3, the coincident definition of the first silicon layer (14) with the second insulating film (16', 18', 20') and second silicon layer (22') would be seriously contemplated by a skilled person in view of the reduced area of the resulting floating gate electrode compared to that of electrode 14" of the alternative with extended first silicon layer disclosed in Figure 6. In particular in view of such increased integration density a skilled person would make practical use of said alternative with said coincident definition. In the Board's view, a skilled person will furthermore expect that oxidation of the aligned first silicon layer (14') proceeds not only from its side walls adjacent to the oxidising atmosphere but

additionally from its layer surfaces adjoining silicon oxide regions 6 and 16' of Figure 3, since in any oxidation step oxygen is able to diffuse through oxide regions. Therefore, contrary to the Appellant's opinion according to paragraph VII-(a) above, a skilled person is able to verify that both conventional alternatives disclosed in document D1 - i.e. the extended and the aligned first silicon layer - can be oxidised from all sides and thereby into a rounded form. For the above reasons, the Board considers that the alternative with aligned first silicon layer disclosed in document D1, in particular at page 7, lines 17 to 21, represents the closest prior art.

1.2 From the closest prior art according to said alternative with aligned first silicon layer disclosed in document D1, there is known (in the wording of Claim 1):

"A method of manufacturing a semiconductor device, using two or more silicon layers (see document D1, 14 and 22 in Figure 2), comprising the steps of:

(a) forming an element isolation region (4 in Figure 1) on a major surface of a silicon substrate (2);

(b) forming a first insulating film (6 in Figure 1) on an element region of said silicon substrate which is isolated by said element isolation region (4);

(c) forming a first silicon layer (14 in Figure 1) doped with phosphorus (see D1, page 6, lines 10 to 13) ... on said first insulating film (6) and said element isolation region (4);

(d) forming a second insulating film (16, 18, 20 in Figure 2) on said first silicon layer (14);

(e) forming a second silicon layer (22 in Figure 2) on said second insulating film (16, 18, 20);

(f) forming an antioxidant film (24 in Figure 2) on said second silicon layer (22);

(g) selectively etching said antioxidant film (24), said second silicon layer (22), said second insulating film (16, 18, 20), and said first silicon film (14) using a mask (26 in Figure 3) having a predetermined pattern (see D1, page 7, paragraph 3);

(h) forming a third insulating film on said wall portions of said first and second silicon layers (14, 22) by selective oxidation using said antioxidant film (24) as a mask (page 8, paragraph 2) ...;

(i) forming a conductive layer (31 in Figure 5) on said second silicon layer (22) and said element isolation region (4), said layer (31) including a portion located on said second silicon layer (22), a portion located on said element isolation region (4), and a portion in contact with said third insulating film (without number between 31 and 14" in Figure 5)."

1.3 Contrary to the Appellant's submission in paragraph VII-(b) above, the following functional definition of the concentration of phosphorous in the first silicon layer (14):

the general feature "high concentration" in step (c) and its definition "wherein said high concentration of phosphorous is contained in said first silicon layer (20) for increasing the speed of oxidation of said (first) silicon layer (20) in step (h) to form said third insulating film (24)".

is additionally disclosed in document D1 for the following reason:

The skilled reader derives from document D1, page 8, paragraph 2 that before the oxidation "exposed gate oxide region 6' is etched back to the silicon surface". This silicon surface belongs to the "P-negative silicon substrate 2" (D1, page 5, paragraph 6). According to document D1, page 8, paragraph 2 during oxidation "the gate oxide 6' is regrown to 45 nm" and "the polysilicon 14" (Figures 4 and 5) oxidises at a faster rate to about 200 nm." Hence, a skilled person derives from this text of document D1 explicitly that the phosphorous doped first silicon layer (14) oxidises four times faster than the usually doped substrate (2). For this reason, in the Board's view, a skilled person is able to recognise that in the conventional method disclosed in document D1 the phosphorous doping of the first silicon layer serves the identical technical purpose as claimed in Claim 1, namely to increase the speed of oxidation of the first silicon layer (i.e. of those layer parts which form a floating gate electrode) for its insulation against the overlying conductive layer. A skilled person is able to foresee, that phosphor doping via the oxidation speed increase contributes as well to the rounding effect mentioned in paragraph VII-(a) above.

It is not immediately evident to the skilled person that the numerical value of the phosphorous concentration disclosed in the present application (see paragraph VII-(c) above) is wrong. Therefore, this error cannot be corrected under Article 88 EPC and for this reason has no influence on the decision to be taken.

1.4 Hence, the subject-matter of Claim 1 is distinguished from the method disclosed in document D1 exclusively by the functional definition of the thickness of the third insulating layer, i.e. by the claimed feature:

said third insulating film "having such a thickness as presents a withstand voltage of said semiconductor device from decreasing".

This means that the objective problem underlying Claim 1 remains to avoid a decrease of the withstand voltage of the third insulating film (i.e. of the insulation between a floating gate and a conduction line). In the Board's view, any deficiencies in time stability of this withstand voltage will be easily noticed by a skilled person during practical use of the conventional device. For this reason, the objective problem does not contribute to an inventive step underlying the subject-matter of Claim 1. Solving this problem by an appropriate thickness represents in the Board's view a routine dimensioning of the duration of the conventional oxidation step disclosed in document D1, page 8, paragraph 2.

2. For the reasons set out above in paragraphs 1.1 to 1.4, Claim 1 does not involve an inventive step and is not allowable pursuant to Articles 52(1) and 56 EPC. Claims 2 to 9 fall because of their dependence on Claim 1.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer G. D. Paterson