

Internal distribution code:

- (A) [] Publication in OJ
(B) [] To Chairmen and Members
(C) [X] To Chairmen

D E C I S I O N
of 15 June 1994

Case Number: T 0139/93 - 3.5.2

Application Number: 88480011.1

Publication Number: 0339165

IPC: H03K 19/017

Language of the proceedings: EN

Title of invention:

GaAs MESFET logic circuits including push pull output buffers

Applicant:

International Business Machines Corporation

Opponent:

-

Headword:

-

Relevant legal norms:

EPC Art. 56

Keyword:

"Inventive step (yes, after amendment)"

Decisions cited:

-

Catchword:

-



Europäisches
Patentamt

European
Patent Office

Office européen
des brevets

Beschwerdekammern

Boards of Appeal

Chambres de recours

Case Number: T 0139/93 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 15 June 1994

Appellant: International Business Machines
Corporation
Old Orchard Road
Armonk, N.Y. 10504 (US)

Representative: Klein, Daniel Jacques Henri
Compagnie IBM France
Département de la Propriété Intellectuelle
F-06610 La Gaude (FR)

Decision under appeal: Decision of the Examining Division of the
European Patent Office dated 31 August 1992
refusing European patent application
No. 88 480 011.1 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R.E. Persson
Members: A.G. Hagenbucher
W.J.L. Wheeler

Summary of Facts and Submissions

I. The present appeal contests the decision of the Examining Division refusing the Appellant's European patent application No. 88 480 011.1. The reason given for the refusal was that the subject-matter of Claim 1 then on file did not involve an inventive step having regard to the following prior art document:

D1: EP-A-0 249 287

and general knowledge.

With respect to the dependent claims reference was also made to

D2: EP-A-0 237 094.

II. In response to objections of the Board, the Appellant filed new claims and amendments to the description and drawings.

III. Independent Claim 1 is now worded as follows:

"1. A high speed logic circuit with improved output driving capability and reduced power consumption of the type including:

(1) a determining logic block (DA) provided with a plurality of logic input terminals (I1, ...) driven by corresponding input logic signals (E1, ...) to perform a determined logical function (F); said logic block (DA) being coupled between at least first and second supply voltages (VH, VD) and supplying first and second output

signals (S1, S2) complementary and substantially simultaneous to each other, at first and second output nodes (13, 14); and,

(2) at least a first output buffer (PP21) comprised of an active pull-up device (T13) receiving said first output signal (S1) and a passive pull-down device (T14) coupled in series intermediate third and fourth supply voltages (at nodes 12, 15);

said logic circuit being characterized in that:

said first output buffer (PP21) further includes an active pull down means (T20) connected in parallel with said pull down device (T14) driven by said second output signal (S2) to ensure a push pull operation of said first output buffer and supply a first circuit output signal (A1) at the common node between said active pull up device (T13) and pull down means (T20); wherein said pull down means is driven by said second output signal (S2) through a first intermediate buffer (IB22) of the source follower type coupled between said third and fourth supply voltages and wherein said first intermediate buffer is comprised of an active pull up device (T24) driven by said second output signal (S2) and a passive pull down device (T25) whose common node is connected to the active pull down means (T20) of said first output buffer (PP21)."

IV. According to the Examining Division's opinion, D1 disclosed a buffer circuit suitable for high-speed logic circuits such as indicated in the preamble of Claim 1. It consisted of a first output buffer including an active pull-down means (T₁₀) connected in parallel with a passive pull-down device (Z₁). The active pull-down means (T₁₀) was driven by a second output signal at node 2 to ensure a push-pull operation of said first output

buffer and supply a first circuit output signal (S_2) at the common node between an active pull-up device (T_{11}) and the pull-down means (T_{10}).

Differential amplifier T_1 , T_2 , R_1 to R_3 of D1 corresponded to the determining logic block DA of the present invention. Remaining features were known from the prior art as shown in Figure 1 of the present application. Hence, the subject-matter of Claim 1 then of file was obvious.

V. According to the Appellant the present invention started from prior art shown in Figure 1 of the present application which had a plurality of logic input terminals and performed logic functions. In contrast thereto D1 concerned a differential sense amplifier to sense and amplify small complementary analog signals generated on the bit lines of a memory cell column. According to new Claim 1 filed during the appeal proceedings, the pull-down means (T_{20}) was driven by a second output signal through a first intermediate buffer IB22 of a certain type whereas output buffer (T_{10}), (T_{11}), (Z_1) of D1 was driven by the second output signal on point 2 through a diode (T_2) which did not allow a quick operation.

VI. The Appellant requested that the decision of the Examining Division be set aside and a patent be granted on the basis of the following documents:

Claims: 1 to 6 received on 4 May 1994 with letter of 29 April 1994;

Description: pages 1, 4 to 6, 13, 14 and 19 as originally filed,
pages 2, 3, 7a, 9, 10, 12, 17, 18 received on 4 May 1994 with letter of 29 April 1994,
page 7 received on 17 January 1994 with letter of 10 January 1994,
pages 8, 11, 15 and 16 received on 20 April 1994 with letter of 13 April 1994;

Drawings: sheets 1/3, 2/3 as originally filed,
sheet 3/3 received on 14 May 1994 with letter of 6 May 1994.

Reasons for the Decision

1. The appeal is admissible.
2. The amendments made to the documents (claims, description and drawings) comply with the requirements of Article 123(2) EPC. All the features in present Claim 1 can be found in original Claims 1 to 3 in conjunction with the description of Figures 2 to 5.
3. None of the cited documents nor the prior art shown in Figure 1 of the present application discloses all the features of the subject-matter defined in present Claim 1. Since novelty is not in dispute, the issue to be decided in the present case is whether the subject-matter of Claim 1 is still objectionable for lack of inventive step.

4. *Closest prior art and problem*

The closest prior art is the circuit described with reference to Figure 1 of the present application. This high-speed logic circuit has all the features indicated in the preamble of Claim 1. As explained on pages 6 and 7 of the present description, this prior art circuit has the drawbacks of dissipating large power and of asymmetric operation which introduces uncertainties in delay and transition times. As explained on pages 8 and 15 of the description, the present invention solves the problem of improving the speed, symmetrisation and reducing power consumption of the high-speed logic circuit shown in Figure 1.

5. The present invention solves this problem by means of a push-pull output buffer design which is controlled by the output signal through an intermediate buffer (IB22).

6. The circuit known from D1 differs from the claimed subject-matter first of all by the input signals. It uses, however, similar to the present invention, a push-pull output buffer design with a load (Z_1) parallel to active pull-down means (T_{10}) in order to calibrate the output signal (S_2) as regards amplitude and switching time. The invention makes use of this known feature in connection with a high-speed logic circuit as known according to Figure 1 of the present application. Whereas according to D1 this output buffer design is used in a differential sense amplifier that senses the binary content of a selected memory cell, the present invention concerns a high-speed logic circuit. A further major difference exists in the control of the active pull-down means. According to present Claim 1 the active pull-down means is driven by the second output signal (S_2) through a first intermediate buffer (IB22) of a source follower type comprising an active pull-up device

driven by said output signal and a passive pull-down device whose common node is connected to the active pull-down means of said first output buffer. According to D1 the active pull-down means is driven by the output signal through a passive diode (D_2) which is less favourable for a quick control than the active intermediate buffer (IB22) of the present invention.

The argument of the Examining Division in paragraph 4.1 of the communication dated 17 June 1991 that the provision of such an intermediate buffer was obvious in view of Figure 3 of D2 (T_{10} , T_{20}) is not convincing because the construction of that buffer is different from the construction of the intermediate buffer (IB22) as recited in Claim 1, and moreover it is not used in the same context.

The Board, therefore, comes to the conclusion that the subject-matter of Claim 1 cannot be derived in an obvious manner from the documents cited by the Examining Division and general knowledge and must accordingly be seen as involving an inventive step as required under Articles 52(1) and 56 EPC.

7. In the opinion of the Board, independent Claim 1, together with the dependent Claims 2 to 6 and the revised description and drawings adapted thereto, can form the basis for granting a patent.

Order

For these reasons, it is decided that:

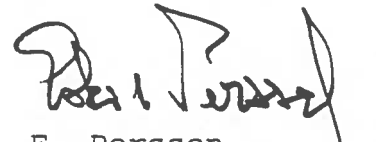
1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a patent on the basis of the documents as defined in paragraph VI above.

The Registrar:



M. Kiehl

The Chairman:



E. Persson

