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D E C I S I O N
of 5 September 1994

Case Number: T 0362/93 - 3.5.2

Application Number: 89306347.9

Publication Number: 0349205

IPC: H03K 5/24

Language of the proceedings: EN

Title of invention:
Differential analog comparator

Applicant:
AT&T Corp.

Opponent:
-

Headword:
-

Relevant legal norms:
EPC Art. 54, 56

Keyword:
"Novelty - yes, after amendment"
"Inventive step - yes, after amendment"

Decisions cited:
-

Headnote/Catchword:
-

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Case Number: T 0362/93 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 5 September 1994

Appellant: AT&T Corp.
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Representative: Buckley, Christopher Simon Thirsk
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 4 December 1992 refusing European patent application No. 89 306 347.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. E. Persson
Members: W. J. L. Wheeler
M. R. J. Villemin

Summary of Facts and Submissions

I. The Appellant filed an appeal against the decision of the Examining Division to refuse the European patent application No. 89 306 347.9. The reason given for the refusal was that the subject-matter of Claims 1 and 9 lacked novelty having regard of the following prior art:

D1: IBM Technical Disclosure Bulletin, Vol. 16, No. 10 March 1974, pages 3227 to 3228;

or:

D2: US-A-3 870 966.

II. In reply to a communication of the Board, the Appellant filed a new set of Claims 1 to 11, a new page 2 and a new figure 1 with a letter dated 9 June 1994. Claim 9 was replaced by a revised version, received 27 July 1994.

III. Claims 1 and 9 now read:

"1. An analog comparator formed on an integrated circuit for comparing a first voltage input to a second voltage input, comprising

a first gain stage (22) having an input, an output and first and second power terminals, the corresponding power terminals coupling to first and second buses, and the input coupling to the first voltage input of the comparator; and

a second gain stage having an input, an output and first and second power terminals, the corresponding power terminals coupling to the first and second buses, and the input coupling to the second voltage input of the comparator;

CHARACTERIZED BY

a first current mirror (40) having a transistor (48) with an output node for coupling a first current to the first bus (32); and

a second current mirror (50) having a transistor (54) with a node for coupling a second current from the second bus (33);

the second current mirror (50) being responsive to an output current from the first current mirror (40) such that the second current is substantially the same as the first current."

"9. A method of comparing first and second input voltages,

comprising the steps of:

amplifying the first voltage with cascaded gain stages powered by first and second buses; and

amplifying the second voltage with cascaded gain stages powered by the first and second buses;

wherein the first and second buses are powered by respective first and second current mirrors, the first current mirror (40) having a transistor (48) with an output node for coupling a first current to the first bus (32), the second current mirror (50) having a transistor (54) with a node for coupling a second current from the second bus (33), and the second current mirror (50) being responsive to an output current from the first current mirror (40) such that the second current is substantially the same as the first current; and

the amplified first and second voltages are complementary outputs indicating whether the second voltage is greater than or less than the first voltage."

Claims 2 to 8 and Claims 10 and 11 are respectively dependent on Claim 1 and Claim 9.

IV. The Appellant requested that the decision of the Examining Division be set aside and a patent be granted in the present amended form, namely on the basis of the following documents:

Claims:
No. 1 to 8 and 10 and 11 as filed with the letter of 9 June 1994, No. 9 as filed on 27 July 1994;

Description:
Pages 1 and 7 as filed with a letter dated 4 November 1992;
Page 2 as filed with the letter of 9 June 1994; and
Pages 3 to 6 as originally filed;

Drawings:
Sheet 1/2 as filed with the letter of 9 June 1994; and
Sheet 2/2 as filed with a letter dated 11 July 1990.

V. According to the Appellant neither D1 nor D2 disclosed or suggested an analog comparator according to Claim 1 or a method according to Claim 9. These claims were therefore allowable.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

2.1 The present Claims 1 and 9 differ from Claims 1 and 9 considered in the decision of the Examining Division in that it is now further specified that the analog comparator comprises:

- a first current mirror (40) having a transistor (48) with an output node for coupling a first current to the first bus (32);

- a second current mirror (50) having a transistor (54) with a node for coupling a second current from the second bus (33);

- the second current mirror (50) being responsive to an output current from the first current mirror (40) such that the second current is substantially the same as the first current.

2.2 The features specified in the claims were all disclosed in combination in the application documents as originally filed. In the opinion of the Board, the present form of the application does not infringe Article 123(2) EPC.

3. *Novelty*

3.1 It is not in dispute that D1 (figure 1) and D2 (figure 3), which show two equivalent circuits having all the features recited in the preamble of Claim 1, represent the closest prior art. In D1 the first and second gain stages comprise IN 1, T5, T6, OUT 1 and IN 2, T7, T8 and OUT 2 respectively. In D2, the first and second gain stages are amplifiers 40 and 42 respectively. Both the D1 and D2 circuits comprise a first pair of P-type transistors (T1, T2 in D1 and 48, 50 in D2) having their conduction paths coupled between a first supply voltage and a first bus, and a second pair of N-type transistors (T3, T4 in D1 and 60, 62 in D2) having their conduction paths coupled between a second supply voltage and a second bus. In D1 and D2, the first and second transistor pairs, whose gates are respectively connected to the first and second outputs of the first and second

gain stages, are not current mirrors. They are operated as variable impedance circuits responsive to the output signals (OUT 1, OUT 2 in D1; 22a, 22b in D2) to translate the operating potentials in such a sense as to counteract changes in the output signals of the first and second stages and maintain the output signal of each stage approximately centred between said operating potentials (cf. D2, column 4, lines 54 to 58). Hence, the subject-matter of the present Claim 1 is new within the meaning of Article 54 EPC.

3.2 Claim 9 relates to a method of comparing first and second voltages by amplifying the first and second voltages with respective cascaded gain stages powered by first and second buses, powered by respective first and second current mirrors as defined in the characterising part of Claim 1, the amplified first and second voltages being complementary outputs indicating whether the second voltage is greater than or less than the first voltage. Since this method is not disclosed in either of the cited prior art documents D1, D2, the subject matter of Claim 9 is also new within the meaning of Article 54 EPC.

4. *Inventive step*

4.1 Though the decision of the first instance was based on lack of novelty over D1, D2, the Board finds it appropriate in the present circumstances to exercise its powers under Article 111(1) EPC and to consider whether the subject-matter of Claims 1 and 9 involves an inventive step, having regard to the prior art cited in the European search report.

4.2 In the circuits known from D1 (figure 1) and D2 (figure 3) each gain stage receives a common set of two operating potentials which are inter alia a function of

the two variable impedances (48, 50 and 60, 62 in figure 3 of D2; T1, T2 and T3, T4 in figure 1 of D1) and of the two supply voltages. Any noise on the power supplies affects also the operating voltages of the gain stages and thus their outputs.

4.3 Starting from either of the closest prior art documents D1, D2, the problem addressed by the present application can be objectively defined as reducing the susceptibility of the comparator known from D1 (figure 1) or D2 (figure 3) to electrical noise on the power supplies. The Board is satisfied that the above problem is solved by a comparator comprising the features specified in Claim 1.

4.4 None of the prior art documents cited in the European search report suggests that a current mirror connected between a power supply and the corresponding bus powering the gain stages of an analog comparator could be used to isolate the comparator from power supply noise. In the opinion of the Board, neither the teaching of the available prior art nor the general knowledge in the relevant technical field would have made it obvious to the skilled person to arrive at a comparator according to Claim 1. Hence, the subject-matter of Claim 1 involves an inventive step within the meaning of Article 56 EPC.

4.5 For similar reasons, the Board finds that also the subject-matter of Claim 9 involves an inventive step within the meaning of Article 56 EPC.

4.6 The subject-matter of Claims 2 to 8 and Claims 10 and 11, which are respectively dependent on Claims 1 and 9, also involves an inventive step.

5. In the opinion of the Board, the amended application documents meet the requirements of the EPC and therefore a patent can be granted according to the Appellant's request.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent in the following version:

Claims:
No. 1 to 8 and 10 and 11 as filed with the letter of 9 June 1994, received 14 June 1994;
No. 9 as filed on 27 July 1994;

Description:
Pages 1 and 7 as filed with the letter of 4 November 1992, received 6 November 1992;
Page 2 as filed with the letter of 9 June 1994; and
Pages 3 to 6 as originally filed;

Drawings:
Sheet 1/2 as filed with letter of 9 June 1994; and
Sheet 2/2 as filed with the letter of 11 July 1990, received 16 July 1990.

The Registrar: The Chairman:

M. Kiehl E. Persson