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D E C I S I O N
of 22 February 1994

Case Number: T 0444/93 - 3.5.2

Application Number: 87401832.8

Publication Number: 0256935

IPC: G11C 11/56

Language of the proceedings: EN

Title of invention:
Read only memory device having memory cells each storing one of three states

Applicant:
Fujitsu Limited

Opponent:
-

Headword:
-

Relevant legal norms:
EPC Art. 56

Keyword:
"Inventive step - no"

Decisions cited:
-

Catchword:
-

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Case Number: T 0444/93 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 22 February 1994

Appellant: Fujitsu Limited
1015 Kamikodanaka Hakara-ku
Kawasaki-shi
Kanagawa 211 (JP)

Representative: Joly, Jean-Jacques et al
Cabinet Beau de Lomenie
55 rue d'Amsterdam
F - 75008 Paris (FR)

Decision under appeal: **Decision of the Examining Division 067 of the European Patent Office dated 9 December 1992 refusing European patent application No. 87 401 832.8 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: E. Persson
Members: W.J.L. Wheeler
M.R.J. Villemin

Summary of Facts and Submissions

I. The present appeal contests the decision of the Examining Division to refuse Appellant's European patent application No. 87 401 832.8. The reason given for the refusal was that the subject-matter of the claims (as amended during the proceedings before the Examining Division) did not involve an inventive step having regard to the prior art known from the following documents:

D1: EP-A-0 044 978

D2: Tietze-Schenk: "Halbleiter-Schaltungstechnik", 1983, pages 270 to 273.

II. The Appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claims considered by the Examining Division.

III. Claim 1 is worded as follows:

"A read only memory device comprising:

a read only memory cell array (21) having a plurality of memory cells (Q(0,0) - Q(n-1,m-1)) each storing one of three states;

selection means (22) connected to said memory cell array, for selecting a pair of memory cells from said memory cell array simultaneously in accordance with an address signal;

a first sense amplifier (SA1), operatively connected to one of the memory cells of the pair, for producing an output corresponding to the state stored in the one of the pair of memory cells selected by said selection means;

a second sense amplifier (SA2), operatively connected to the other of the memory cells of the pair, for producing an output corresponding to the state stored in the other of the memory cells of the pair selected by said selection means; and

decoder means (23) connected to said first and second sense amplifiers (SA1, SA2) for receiving the outputs of said first and second amplifiers and producing a three bit binary data output (X0, X1, X2) corresponding to the states stored in the pair of memory cells,

characterized in that each said sense amplifier delivers its output on three bits, and said decoder means (23) comprises a read only memory (24) comprised of a matrix of transistors, receiving the three bit output (S0, S1, S2) from said first sense amplifier (SA1) as a column address and the three bit output (S'0, S'1, S'2) from said second sense amplifier (SA2) as a row address, and in that said three bit outputs (S1, S2, S3, S'0, S'1, S'2) which are produced from said first and second sense amplifiers represent whichever state among the said three states is stored by said memory cells, the three bit outputs forming an address whereby the data stored in the matrix is read out to output said three bit binary data (X0, X1, X2)."

Claims 2 to 4 are dependent on Claim 1.

IV. The Appellant argued essentially that the inventors had departed significantly from the teaching of D1 by

(i) providing two sense amplifiers for the respective pair of tri-state cells,

(ii) designing the sense amplifiers so that they delivered the tri-state information of the

corresponding cell in the form of binary logic signals on three corresponding signal lines, and

(iii) choosing the decoder to be of the matrix type so that it could be addressed by the two groups of signal lines, at rows and columns thereof.

The Examining Division had considered these features separately and applied an *ex post facto* analysis that did not take account of the synergy in the invention when considered as a whole. In D1, the sense amplifiers each produced only two binary outputs which were fed to logic circuitry to produce the final three bit output. The outputs of the sense amplifiers were not suitable for addressing a decoding matrix. The matrix decoder was fast, economical and flexible regarding data content.

Reasons for the Decision

1. The appeal is admissible.

2. The Board agrees with the Examining Division that a read only memory device according to the preamble of Claim 1 is disclosed in D1 (EP-A-0 044 978).

3. As pointed out by the Appellant, it is true that in the particular embodiment disclosed in D1, the level decoder shown in Figure 4 comprises logic circuits (35, 36, 37, 38) and sense circuits (31, 32, 33, 34) designed to provide suitable signals (on lines 311, 321, 331, 341) for the logic circuits. However, even though no other level decoder is disclosed, it is clear from D1 that the level decoder can take other forms, see D1, Claim 1, last three lines, and the summary on page 2, second paragraph.

4. It is well known to persons skilled in the art that a ROM comprising a matrix of transistors may be used instead of logic circuits to perform coding and decoding operations. In the opinion of the Board, a person skilled in the art reading D1 would immediately realise that he could use a ROM matrix instead of the logic circuits shown in Figure 4 of D1 and that, as a necessary consequence, the sense amplifiers would have to be adapted to address the columns and rows of the ROM matrix in dependence on which of the three possible states was stored in each cell of the selected pair of memory cells. It would be obvious to him that this required three address lines from each sense amplifier. Proceeding along this obvious path, the skilled person would inevitably arrive at a read only memory device according to the present Claim 1.

5. The Board concludes that although the subject-matter of independent Claim 1 is new, it does not involve an inventive step within the meaning of Article 56 EPC. As found by the Examining Division, this also applies to the subject-matter of dependent Claims 2 to 4 on file. The appeal must therefore be dismissed.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Kiehl E. Persson