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D E C I S I O N
of 16 June 1994

Case Number: T 0535/93 - 3.5.2

Application Number: 86116121.4

Publication Number: 0224206

IPC: G11C 11/00

Language of the proceedings: EN

Title of invention:
Integrated circuit memory

Applicant:
Mitsubishi Denki Kabushiki Kaisha

Opponent:
-

Headword:
-

Relevant legal norms:
EPC Art. 54

Keyword:
"Novelty (no)"

Decisions cited:
-

Headnote/Catchword:

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0535/93 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 16 June 1994

Appellant: Mitsubishi Denki Kabushiki Kaisha
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Representative: Eisenführ, Speiser & Partner
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 27 January 1993 refusing European patent application No. 86 116 121.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R.E. Persson
Members: W.J.L. Wheeler
A.G. Hagenbucher

Summary of Facts and Submissions

I. The Appellant contests the decision of the Examining Division to refuse application No. 86 116 121.4. The reason given for the refusal was that the subject-matter of the claims then on file did not involve an inventive step. The following prior art documents were considered by the Examining Division:

D1: IBM Technical Disclosure Bulletin, Vol. 15, No. 1, June 1972, page 270;
D2: EP-A-0 152 584;
D3: US-A-4 442 345; and
D4: IEEE Transactions on Consumer Electronics, CE-32, No. 3, August 1986, pages 604-607.

II. With a letter dated 19 May 1994, the Appellant filed a single claim to replace all the claims previously on file. The claim reads as follows:

"An integrated circuit memory having a memory function and is formed in one chip or one module, characterized in that said memory function comprises a function that data can be stored nearly permanently and rewriting of the data becomes impossible, and a function that data can be rewritten if necessary."

III. Oral proceedings were held on 16 June 1994. The Appellant argued that the claim was based on the priority document (JP 262870/85) and that therefore D4, which was published after the claimed priority, was no longer relevant. The memory according to the invention had read-only regions, where the stored data could never be changed, and read/write regions. The number of pins on the chip could be reduced by having common power sources for reading and writing and common address lines. The access time of the memory was short. In the

prior art according to D1, D2 and D3, data which was intended to be read-only could be changed, if incorrect control signals were applied.

IV. The Appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claim filed with the letter dated 19 May 1994.

Reasons for the Decision

1. The appeal is admissible.

2. The present claim, unlike the ones decided upon by the Examining Division, is fully supported by the priority document JP 262870/85 and is entitled to the priority date of 22 November 1985. Consequently, D4, which was published in August 1986, does not belong to the prior art and must be left out of account (Articles 89 and 54(2) EPC).

3. D1 (which was cited in the Examining Division's communication dated 4 June 1991 and drawn to the Appellant's attention in the oral proceedings before the Board) carries the title: "256-BIT CHIP FOR 128-BIT LATENT IMAGE STORE" and discloses a semiconductor memory array adapted by the final metallization masking operation to achieve, in one array, both a read-only memory (ROM) and a random-access memory (RAM) capability. It explains that if, in a RAM array, half the RAM cells are converted to ROM cells by changing the interconnections within those cells, leaving the other half in the normal RAM mode, a significant speed advantage can be realised, since the ROM portion of the array is within reach of the CPU of the computer and is perfectly compatible therewith. It is implicit that the

data stored in the ROM cells cannot be rewritten. The memory chip disclosed in D1 falls within the terms of the present claim.

4. It is noted in passing that D2 and D3 also disclose integrated circuit memories having RAM and ROM functions in one chip, falling within the terms of the present claim.

5. Since the subject-matter of the claim forms part of the state of the art according to Article 54(2) EPC, it cannot be considered to be new within the meaning of Article 54(1) EPC and thus it does not meet the requirement of Article 52(1) EPC.

6. The Appellant's arguments cannot prevail over the above finding of lack of novelty, because the claim does not recite any features which are not present in the prior art memory chips for reducing the number of pins, shortening the access time, or preventing changing of data stored in the ROM region in the event of incorrect control signals being applied. Nor does the claim specify distinct ROM and RAM regions.

7. Thus, the Appellant's request cannot be granted and the appeal must be dismissed.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar:

M. Kiehl

The Chairman:

E. Persson