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D E C I S I O N
of 18 April 1996

Case Number: T 0622/93 - 3.4.1

Application Number: 87308978.3

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Title of invention:
MOS semiconductor device

Applicant:
KABUSHIKI KAISHA TOSHIBA

Opponent:
-

Headword:
MOS semiconductor device/K. K. TOSHIBA

Relevant legal provisions:
EPC Art. 54, 56, 84

Keyword:
"Clarity - yes"
"Novelty - yes"
"Inventive step yes (after amendments)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0622/93 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 18 April 1996

Appellant: KABUSHIKI KAISHA TOSHIBA
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 20 January 1993 refusing European patent application No. 87 308 978.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. D. Paterson
Members: R. K. Shukla
Y. J. F. Van Henden

Summary of Facts and Submissions

I. European patent application No. 87 308 978.3 relating to a MOS semiconductor device was refused in a decision of the Examining Division on the grounds that the claims forming the basis of the main and auxiliary requests did not comply with the requirement of clarity pursuant to Article 84 EPC, and that, in so far as the claims could be understood, they did not comply with the requirements of novelty and inventive step (Article 52(1) EPC) having regard to the following prior art document:

D1- IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. ED-33, No. 1, January 1986, pages 140-144.

II. According to the above decision, the term, "maximum operating power supply voltage" in claims 1 and 3 did not clearly define the scope of the claims even when account was taken of the description in the application as filed, and the disclosure in document D1 and the following prior art document,

D2- IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. ED-32, No. 3, March 1985, pages 562-570.

It was also held by the Examining Division that under the assumption that device reliability in the application was measured in the same way as proposed in document D1, page 141, left column, second and third paragraph, and that the maximum operating power supply voltage was comparable with the highest applicable voltage mentioned in document D1, the subject-matter of claim 1 was not novel with respect to the device described with reference to Figure 5 of document D1.

The subject-matter of claim 3 of the main request (corresponding in substance to claim 1 of the auxiliary request) was considered as lacking in inventive step having regard to the device of Figure 5 of document D1.

III. The applicant lodged an appeal against the decision, and filed along with a statement of the grounds of appeal a main request and several auxiliary requests. Oral proceedings were requested in the event that the Board intended to dismiss the appeal.

IV. In its communication pursuant to Article 110(2) and a subsequent communication annexed to summons to oral proceedings, the Board informed the Applicant that the application did not comply with the requirements of clarity and inventive step, and suggested amendments to overcome these objections.

V. The Applicant filed on 5 February 1996 a set of amended claims and amended pages of the description taking into consideration the amendments suggested by the Board, and now requests the grant of a patent on the basis of the following application documents:

Claims: 1 and 2 filed with the letter dated 5 February 1996;

Description: pages 1 to 3, 5 to 8 and 10 to 13 as originally filed;
page 14 as filed with the letter dated 15 May 1992;
page 9 filed with the latter dated 16 October 1995; and
pages 4, 4a filed with the letter dated 5 February 1996;

Drawings: sheets 1/5 and 3/5 to 5/5 as originally filed and
sheet 2/5 as filed with the letter dated 15 May 1992.

VI. In view of the amendments to the application, the oral proceedings scheduled to be held on 15 February 1996 were no longer considered to be necessary and were therefore cancelled.

VII. Claims 1 and 2 of the above request read as follows:

Claim 1:

"A MOS semiconductor device, in operation, having an off state and an on state, comprising a submicron transistor, including a semiconductor substrate (40) of a first conductive type, and capable of being operated by an applied power source voltage, comprising:

a gate insulation layer (46) on the semiconductor substrate (40);

a gate electrode (47) located on the gate insulation layer (46);

single type impurity regions (43) of a second conductive type in the semiconductor substrate (40) and adjacent to the gate electrode (47) and the gate insulation layer (46), said impurity regions (43) respectively defining a source and a drain across which said power-source voltage is applied; and

a channel region (45) extending between said impurity regions (43), beneath said gate insulating layer (46);

characterised in that the maximum power supply voltage V which is applied to the drain during operation of the device is less that 5 volts and is determined by the gate length L in micrometers according to the equation

$V1/1.1 \leq V \leq V1/0.9$
where $V1 = 6.2 \times \sqrt{(L/2)}$ in volts;

Claim 2:

A MOS semiconductor device, in operation, having an off state and an on state, comprising a submicron transistor, including a semiconductor substrate (10) of a first conductive type, and capable of being operated by an applied power source voltage, comprising:

a gate insulation layer (16) on the semiconductor substrate (10), the thickness of the gate insulation layer (16) being a function of gate delay time and the impurity density of the substrate (10) being a function of punch-through voltage;

a gate electrode (17) on the gate insulation layer (16);

first impurity regions (14) of a second conductive type in the semiconductor substrate (10) and adjacent to the gate electrode (17) and the gate insulation layer (16);

second impurity regions (13) of a second conductive type, having a higher concentration than that of the first impurity regions (14), in the semiconductor substrate (10) and adjacent to the first impurity regions (14), said second impurity regions (13) respectively defining a source and a drain across which said power source voltage is applied; and

a channel region (15) between said first impurity regions (14), beneath said gate insulation layer (16);

characterised in that the maximum power supply voltage V which is applied to the drain during operation of the device is less that 5 volts and is determined by the gate length L in micrometers according to the equation

$V1/1.1 \leq V \leq V1/0.9$
where $V1 = 8.2 \times \sqrt{(L/2)}$ in volts;
the gate insulation layer has an electric field in the range of 3 to 3.5 MV/cm applied thereto."

Reasons for the Decision

1. *Amendments*

In relation to claim 1 as filed, the present claim 1 under consideration has been amended so that

(i) it relates to a MOS semiconductor device **in operation**,

(ii) the power source voltage V is stated to be " the maximum power supply voltage V which is applied to the drain during the operation of the device",

(iii) "L" designates the gate length, and not the length of the gate electrode,

(iv) the voltage range for the supply voltage V, in terms of the gate length L in micrometers, is defined as follows:

$V1/1.1 \leq V \leq V1/0.9$, where $V1 = 6.2 \times \sqrt{(L/2)}$ in volts, and

(v) an electric field in the range of 3 to 3.5 MV/cm is applied to the gate insulation layer.

Claim 2 also contains the same amendments as above in relation to claim 3 as filed, with the exception that in claim 2, $V1 = 8.4 \times \sqrt{(L/2)}$. Additionally, the

claim requires that (vi) the thickness of the gate insulation is a function of gate delay time and the impurity density of the substrate is a function of punch-through voltage.

The above amendments (i) and (ii) are by way of clarification of the term, "the maximum operating power supply voltage", and find support in the original description, for example, on page 6, lines 7 to 21. Similarly, the amendment (iii) is supported by the original description page 6, lines 14 and 18, and Figure 4 of the application. As to the relationships $V1 = 6.2 \times \sqrt{(L/2)}$ and $V1 = 8.4 \times \sqrt{(L/2)}$, these are disclosed on page 11, lines 25 and 22 of the original description. The amendment under item (v) is disclosed in claims 2 and 3 as originally filed. Amendments specified in item (vi) are supported by the description on page 8, lines 8 to 10 and page 10, line 23 to page 11, line 8.

The description has been amended so as to be in conformity with the subject-matter of claims 1 and 2. In Figure 3 of the drawing, the box (e) has been deleted so that the flow diagram of the Figure is consistent with its description on page 9, lines 10 to 18 as filed.

In view of the above, the Board is satisfied that the application as amended complies with the requirements of Article 123(2) EPC.

2. *Clarity*

Claims 1 and 2 now relate to a MOS device in operation, and the maximum operating power supply voltage V is not a device parameter as in the claims forming the basis of the decision, but is the voltage actually applied to the drain during the operation of the device. This power

supply voltage V lies within a range which is determined by the gate length L in micrometers of the device, as stated in the claim. In the Board's judgment, therefore, the amended claims comply with the requirement of clarity according to Article 84 EPC.

3. *Novelty*

The prior art MOS semiconductor device described with reference to Figure 1 on page 140, right hand column, "II. DEVICE FABRICATION", of document D1 comes closest to the MOS device according to claim 1, and discloses a sub-micron MOS field effect transistor as defined in pre-characterising part of claim 1. Moreover, as shown for the curve for arsenic in Figure 5 of the document, the highest applicable voltage for a gate length L of about 0.9 µm is approximately 4.4 volts. The maximum power supply voltage V1/0.9 which is applied to the drain of the MOS device according to claim 1 is approximately 4.21 volts for the same gate length. The thickness of the gate insulation employed in the prior art device is disclosed to be 23 nm (see "Device Fabrication", second paragraph) and the highest applicable voltage for various effective channel lengths is derived under the condition Vg = Vd (see page 142, left-hand column, lines 4 to 7), so that for Vd = 4.4 volts, the electric field applied to the gate insulation amounts to about 1.9 MV/cm. Thus, the prior art device does not disclose electric field applied to the gate insulation in the range claimed in claim 1. The subject-matter of claim 1 is therefore novel.

Similarly, for a gate length of 0.5 µm, the curve for LDD type device of Figure 5 of document D1 gives a value of about 5 volts for the highest applicable voltage. Under the Vg = Vd condition, therefore, the electric field applied to the gate insulation is about

2.17 MV/cm. Thus the range for the applied electric field for the gate insulation as claimed in claim 2 is not disclosed in document D1, and consequently, the subject-matter of claim 2 is new.

4. *Inventive step*

4.1 The present application relates to the operation of a sub-micron MOS field effect transistor, based on a new design rule in the scaling down of the transistor to a sub-micron channel length. When the channel length is reduced below 1.0 µm, the device reliability is known to suffer due to hot carriers generated by the presence of intense electric field in the channel region adjacent to the drain. The reduction in the power supply voltage in order to reduce the electric field, however, deteriorates the speed of the device (see page 2, line 13 to page 3, line 6 and page 3, lines 7 to 21 of the application as filed).

As submitted by the appellant in the statement of grounds and as disclosed in the application (see page 3, line 22 to page 4, line 2), the present invention addresses the technical problem of providing a MOS device which has the shortest channel length compatible with high reliability for a given maximum operating voltage whilst maintaining maximum speed of operation.

4.2 The results of the experiments carried out with various drain structures, as reported in Figure 5 of document D1, show that hot carrier effect can be avoided by reducing highest applied voltage when channel length is reduced. However, on plotting the curves between the channel length and the upper limit of the maximum power supply voltage, i.e. V1/0.9, according to the relationships specified in claims 1 and 3, respectively, on the curves for arsenic and the LDD structure of

Figure 5, it can be seen that for power supply voltage less than 5 volts, the curves according to the claims are steeper than those of Figure 5. According to the scaling down rule of the present invention, therefore, for a predetermined channel length, the power supply voltage applied to the drain is considerably smaller than that according to the curves of Figure 5.

As can be seen from the flow chart of Figure 3 in the application, in an overall optimisation, it is also necessary to select gate insulation thickness with a view to achieving an optimum gate delay time. In the invention as claimed, therefore, the relationship between the channel length and the maximum operating power supply voltage applies only for those transistors where the gate insulation thickness has been chosen so as to have an electric field within the range specified in the claims.

In view of the above, the Board agrees with the appellant that the above simultaneous optimisation of gate insulation thickness and the maximum operating power supply voltage for a given sub-micron channel length with a view to achieving a high reliability and high device speed is not derivable from the disclosure in document D1.

4.3 Document D2 mainly deals with the design of a Double-Diffused Drain MOSFET to reduce hot-carrier emission. The document does not disclose any optimisation of the maximum operating power supply voltage or the gate insulation thickness with a view to improving the reliability and the device speed.

Also, the remaining prior art documents cited in the European search report are not relevant to the question of inventive step.

4.4 For the foregoing reasons, in the Board's judgment, the subject-matters of claims 1 and 2 are not obvious having regard to the cited prior art, and the claimed subject-matters therefore involve inventive step.

Order

For these reasons it is decided that:

1. The decision of the first instance is set aside.

2. The case is remitted to the first instance with the order to grant a European patent on the application documents specified in item V above.

The Registrar: The Chairman:

M. Beer G. D. Paterson