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D E C I S I O N
of 9 November 1995

Case Number: T 0683/93 - 3.5.1

Application Number: 86109447.2

Publication Number: 0208319

IPC: G06F 13/16

Language of the proceedings: EN

Title of invention:
A system for providing selective interconnection between a plurality of ports

Applicant:
WANG LABORATORIES INC

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0683/93 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 9 November 1995

Appellant: WANG LABORATORIES INC.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 3 March 1993 refusing European patent application No. 86 109 447.2 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: A. S. Clelland
G. Davies

Summary of Facts and Submissions

I. European patent application No. 86 109 447.2, filed on 10 July 1986 claiming a priority of 12 July 1985 and published under No. 0 208 319, was refused by a decision of the Examining Division issued on 3 March 1993.

The reason given for the refusal was that the subject-matter of the then current independent claim lacked an inventive step having regard to the disclosure of the following prior art document:

D1: US-A-3 916 380.

II. On 28 April 1993 the Applicant lodged an appeal against this decision and paid the appeal fee. On 2 July 1993 a statement setting out the grounds of appeal was filed, requesting grant of a patent on the basis of a newly formulated independent claim.

In response to communications pursuant to Article 110(2) EPC raising objections under Articles 123(2), 84 and 56 EPC, the Appellant submitted further amendments to the claims. At oral proceedings held on 9 November 1995, claims originally submitted on 2 October 1995 as the basis of an auxiliary request were amended in response to comments from the Board and, together with appropriate changes to the description, were made the subject of a single request for grant of a patent.

III. The Appellant's single request is the grant of a patent on the basis of the following documents:

Claims: 1 to 4 filed in the oral proceedings;

Description: pages 1 to 3, 5 to 22 and 24 to 35 as originally filed; insert for page 4 submitted 2 July 1993; and pages 4, 23 and 36 filed at the oral proceedings;

Drawings: sheets 1 to 10 as originally filed.

IV. The independent claim reads as follows:

"A connection system (40) comprising a switch controller (50) and at least one interface module (60), for providing selective interconnection between a plurality of ports (26) adapted for transferring data to requesting devices (workstation computer WC 12) and a plurality of channels (28) adapted for connection to data retrieval devices (mass storage devices MSD 30), each channel (28) including a command line (CMD) for carrying command signals, a response line (RSP) for carrying response signals, a clock line (VCL) for carrying clock signals and a data line (VD) for carrying data
characterized by

- a first bus (52; 102, 108) including address lines (108) and data lines (102) interconnecting the switch controller (50) and the at least one interface module (60) for controlling operation of multiplexing switches (206, 208, 210, 211) included in the at least one interface module (60), and

- a second bus (54) interconnecting the switch controller (50) and the at least one interface module (60) and providing the plurality of channels (28) for connection to the data retrieval devices (30), wherein

- the second bus (54) includes

- a bit serial data line (VD0-VD15), a bit serial data clock line (VCL0-VCL15), a bit serial command line (CMD0-CMD15) and a bit serial response line (RSP0-RSP15) for each channel, and

- the at least one interface module (60) includes a plurality of ports (26) for connecting to the requesting devices (12), wherein - each port (26) includes a bit serial command line (CMD), a bit serial response line (RSP), a bit serial data line (VD) and a bit serial clock line (VCL),

- the interface module (60) further includes:

- multiplexing control logic (232, 260, 262) connected to the ports (26) for receiving connection requests from the requesting devices (12) for connection to a channel (28) and responsive to said connection requests to selectively control connections between the command, response, data and clock lines of the ports (26) and the command, response, data and clock lines of the channels (28) through the multiplexing switches (206, 208, 210, 211) to provide the requested connections between the ports (26) and channels (28), and - the switch controller (50) includes

- a processor (100) and control circuitry connected to the first bus (52, 106, 108),

- wherein the switch controller (50)

- is responsive to a command to establish a connection between a requesting device (12) and a

data retrieval device (30) to establish a connection between the corresponding port (26) and channel (28) through the multiplexing switches (206, 208, 210, 211),

- and is thereafter responsive only to a command appearing on the command line of the connected port to terminate the connection between the requesting device (120) and the data retrieval device (30)."

V. The Appellant's arguments in support of the patentability of the subject-matter of the independent claim may be summarised as follows:

The connection system of the invention had been conceived to carry out a particular task. It should connect a relatively small number of mass storage devices to a variable, relatively large, number of workstation computers requiring large amounts of data (typically image data) to be transferred at high speed. Data would flow essentially in one direction, from the mass storage devices to the workstations. The invention was specifically designed to support this asymmetry in an elegant and cost-effective way. The system of document D1 on the other hand was simply designed for two-way connection of computers in a symmetrical fashion. This fundamental difference led to a number of features of the invention, reflected in the main claim, which it would not be obvious to add to the system of D1.

The Appellant drew attention to three areas in which the claimed subject-matter was considered different from the disclosure of D1. Firstly, the topology of D1 was said to be different from that of the invention; D1 was designed explicitly for two-way connections and was in effect a crossbar switch making use of reflection.

Because of its symmetrical nature D1 required the presence not only of multiplexers but demultiplexers, the control logic being such that only a limited number of parallel paths was feasible at any one time. The system could therefore not be expanded. Secondly, it was argued that the internal structure of D1 was quite different to that claimed. Claim 1 required the presence of a first bus, including address and data lines, interconnecting the switch controller and interface modules for controlling operating of the multiplex switches; D1 on the other hand, as could be seen from Figure 10, provided point-to-point wiring between the controller and the multiplexer/demultiplexer pairs and only allowed three to be addressed at any one time. Only a fixed number of interface controller cards could therefore be used.

Thirdly, a connection in the invention comprised four lines VD, VCL, CMD and RSP. CMD and RSP were differently routed as compared with VD and VCL. Only the command and response lines CMD and RSP needed to be connected to the switch controller, since connection requests could only appear on the CMD line. This permitted a much higher speed connection on the data lines VD and VCL than would have been possible if these lines too were routed via the switch controller. Nonetheless, the CMD and RSP lines were so connected that they also made a full path through the connection system. This was essential to allow the cascading of such systems.

The disclosure of D1 was not clear on these points, and appeared contradictory. It seemed from Figures 7 and 8 and column 6 line 54 to column 7 line 7 that an RSP signal was generated by the switch controller, in which case Figure 6 was wrong and there was no full path for the RSP signal through the connection system. Further, when requesting a connection, while the request was

signalled on line REQ, the required address was communicated on lines 191 (see Figures 9 and 10). There were two interpretations of this: either lines 191 were the data lines from a port, in which case it could not be said that the data and command routes were separated, or these lines were completely new and simply not shown in Figures 5 and 6. In the latter case there was no indication of a route through the connection system for the command lines. The line REQ did not on its own constitute a command line as required by the claimed invention.

Reasons for the Decision

1. *Admissibility*

The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. *Amendments*

The Board is satisfied that the amendments to the patent application do not contravene Article 123(2) EPC.

3. *Inventive step*

3.1 The only issue to be decided is whether the subject-matter of Claim 1 involves an inventive step.

The application is concerned with a problem which arises in transferring data from mass storage devices to computer workstations. Cost constraints require that the limited number of mass storage devices be shared out amongst a greater number of workstations, necessitating some form of switching in order to connect an individual

work station to a mass storage device. When the stored data is graphic or pictorial in nature, very high data rates are required. According to the application this has in the past been achieved by connecting each workstation to a central computer such as a mainframe, which is in turn connected to the mass storage devices. Such a system is said to give rise to the problem that because of the time-sharing nature of the services provided by the central computer, data rates are comparatively low and system performance is easily degraded when the central computer is accessed by a number of workstations simultaneously.

3.2 This problem is said to be overcome by the provision of a connection system which interfaces the workstations with the mass storage devices by way of interface modules. Each interface module has one set of ports for connection to requesting devices such as workstations and is connected by way of a bus to a second set of ports, referred to in the application as channels, which in turn connect with the mass storage devices. The interface modules include multiplexing devices controlled by a switch controller by way of a bus and which serve to provide connections between selected ports and channels; the connection path comprises four separate bit-serial lines, namely a command line, a response line, a data line and a clock line. Once a connection has been established by way of the command and response lines, all further commands are passed through the interface module unless the command is one requiring termination of the connection; thus a plurality of devices can be cascaded to increase the number of available ports or channels, commands being passed through the first such device after it is set up and thus enabling the next device in line to be addressed.

3.3 The application was refused by the first instance on the ground that the subject-matter of the then Claim 1 lacked an inventive step having regard to the disclosure of D1. Although not explicitly concerned with connecting workstations to mass storage devices, this document discloses a switching controller for enabling a plurality of computers to be interconnected. Although at first sight the drawings disclose the provision of a plurality of input and output ports, only a single set of ports is present, data which is inputted at one port being reflected to another port; separate input and output ports are apparently only shown in Figures 4 and 6 to illustrate the path of data through the switch. Referring to Figures 4 and 6, the connection system comprises a switch controller in the form of control logic 41 and a plurality of interface modules, 43 and 45, 47 and 49, and 51 and 53; these modules provide selective interconnection between a plurality of ports 27 to 37, adapted for transferring data to requesting devices, and a plurality of output ports or channels adapted for connection to source devices. The source devices are other computers, i.e. data retrieval devices as required by Claim 1. Each channel can be seen from Figure 5 to include a command line 95, REQI, for carrying command signals, a response RSP for carrying response signals, a clock line RDY for carrying clock signals and a plurality of data lines D1 to D8 for carrying data. The features of the preamble of Claim 1 are accordingly known from D1.

3.4 Turning now to the characterising features of Claim 1, the claim requires a first bus including address and data lines interconnecting the switch controller and the at least one interface module for controlling operation of multiplexing switches included in the module. It was argued by the Appellant that this feature was not known from D1, which controlled the individual multiplexers

and demultiplexers by means of point-to-point wiring between the control logic and the individual mutliplexers and demultiplexers. The Board accepts that this analysis of D1 is correct but considers that no invention would be involved in joining all the devices by means of a single bus rather than by point-to-point wiring; in this case it would be necessary to provide address lines and data lines as specified in Claim 1. Although the Board accepts that the network topology of D1 differs from that of the invention, this is not brought out in any way in the claims. In particular, Claim 1 does not exclude the use of demultiplexers. The claim goes on to require a second bus interconnecting the switch controller and at least one interface module and providing the plurality of channels for connection to the data retreval devices. Although this feature is not explicitly disclosed by D1 the Board considers that the manner in which the individual ports are connected to a plurality of multiplexers and demultiplexers in D1 and by way of lines 73, 75 and 77 to the control logic can be considered as constituting a bus in the same sense as is used in the claim, in that the output ports shown on the right hand side of Figure 4 are each connected to a plurality of demultiplexers, a plurality of devices thus being connected to a single line; in the Board's view the second bus of Claim 1 does nothing more than this.

3.5 The claim goes on to state that the various lines constituting the signal path between a port and a channel - the command, response, clock and data lines - are serial in nature. It was argued by the Appellant that if the skilled person were to adapt the D1 arrangement to serial lines he would have no reason to provide the four lines used in the invention, which enabled the data requested from a mass storage device to be transferred over a separate path to that used for

control data such as commands and responses; it was thus possible to have two different speeds, one for the mass storage device data, and another, slower, speed for the control data. Another advantage arising from this, it was argued, was that the switch controller, once set up, could be made transparent to commands to carry out a commanded connection so that a plurality of controllers could be cascaded. This feature is brought out in the closing four lines of the claim, which state that after a connection is established the controller is responsive only to a termination command on the command line.

3.6 Although the mere substitution of the parallel, i.e. byte-serial bus by a bit-serial bus would appear to be a non-inventive design option, the Board has concluded that the implementation claimed does indeed give rise to the twin advantages of a potentially high data rate and the ability to cascade devices. D1 provides a parallel arrangement of eight data lines and corresponding handshaking lines. In such an arrangement two separate paths for high-speed data and control data are not possible. Although D1 provides various lines analogous to lines used in the invention, as recognised in the claim preamble, it is equally apparent that no addressing is performed by means of these lines. It can be seen from Figures 9 and 10 of D1 that the connections between the ports are determined by data on lines 191 said to come from the port itself. The description of D1 nowhere indicates how this data is derived but the Board notes that in Figure 4 the lines 73, 75, 77, taken from the path between the multiplexer and demultiplexer in each pair, supply data to the control logic. It therefore appears likely that the data lines also serve as address lines, so that the data and control functions are not separated in the manner of Claim 1. The claim provides separate bit-serial (i.e. data carrying) lines from the mass storage device to the requesting device

for responses and for the requested data, thus allowing a higher-speed line to be used for the requested data. There is nothing to be found in the teaching of D1 which would lead the skilled person converting the parallel system of D1 into a bit-serial system to provide these separate lines. Further, there is no indication in D1 of the desirability of cascading devices, so that there is no incentive for the skilled person to provide the claimed features which make cascading possible.

3.7 The Board does not consider that the skilled person would be led to modify the D1 data line arrangement so as to arrive at the claimed arrangement. Accordingly, the subject-matter of Claim 1 is considered to involve an inventive step.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent in accordance with the Appellant's request.

The Registrar: The Chairman:

M. Kiehl P. K. J. van den Berg