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# D E C I S I O N
## of 18 December 1997

**Case Number:** T 0127/94 - 3.5.1

**Application Number:** 87116725.0

**Publication Number:** 0267612

**IPC:** G06F 9/46

**Language of the proceedings:** EN

**Title of invention:**
Timer/counter using a register block

**Applicant:**
NEC Corporation

**Opponent:**
-

**Headword:**
-

**Relevant legal provisions:**
EPC Art. 56

**Keyword:**
"Inventive step (yes)"

**Decisions cited:**
-

**Catchword:**
-

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Case Number: T 0127/94 - 3.5.1

# D E C I S I O N
## of the Technical Board of Appeal 3.5.1
## of 18 December 1997

**Appellant:** NEC Corporation
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Minato-ku
Tokyo (JP)

**Representative:** Glawe, Delfs, Moll & Partner
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**Decision under appeal:** **Decision of the Examining Division of the European Patent Office posted 17 September 1993 refusing European patent application No. 87 116 725.0 pursuant to Article 97(1) EPC.**

**Composition of the Board:**

**Chairman:** P. K. J. van den Berg
**Members:** R. R. K. Zimmermann
V. Di Cerbo

## Summary of Facts and Submissions

I. The appeal was lodged against a decision of the examining division, dated 19 September 1993, refusing the European patent application No. 87 116 725.0 (publication No. 0 267 612). The application claiming a priority date of 12 November 1986 was filed on 12 November 1987.

II. According to the examining division, the subject-matter of claim 1 lacked an inventive step essentially in view of document D1 (US-A-4 024 510) considered as the closest prior art document and document D2 (I.E.E.E. ELECTRO, vol. 8, suppl. 1983, pages (4/3) 1-7; PAWLOSKI: "Continuing the evolution of high performance single chip microcontrollers"). As alleged in the decision, even the general teaching in document D2 would lead the skilled person to the invention since CAM cells were mainly concerned with the problem of reducing the chip area and allowed, in one unit, to store and compare values supplied to the CAM.

The European search report mentions following further documents:

(D3) EP-A-0 175 603

(D4) US-A-3 633 181

(D5) US-A-4 220 990

III. The applicant filed a notice of appeal on 16 November 1993, requesting reversal of the decision and grant of the patent. The fee for appeal was paid on the same day. A written statement setting out the grounds of appeal and including amended application documents followed on 14 January 1994.

IV. The present decision is issued on the basis of the following requests submitted by the appellant on 22 July 1997:
According to the **main request**, the contested decision should be set aside and a patent granted with the following documents:

**Description**:
Pages 2, 6, 11 - 16, 18 as originally filed.
Pages 4, 8, 17 and 19 as filed on 14 January 1994.
Pages 1, 3, 4a, 7, 9, 10 as filed on 26 February 1997.
Page 5 as filed on 22 July 1997.

**Claims**:
No. 1 to 3 as filed on 22 July 1997.

**Drawings**:
Sheets 1/6 - 6/6 as originally filed.

As a subsidiary measure, oral proceedings should be held.

Claim 1 according to the main request reads as follows:

"1. A timer/counter comprising:
an operation controller (36) coupled to a data bus (20) for receiving a control information for generating control signals for a selected operation mode of the timer/counter,
a register block (10) coupled to an internal bus (18) including
a plurality of count registers (14A-14D),
a corresponding number of timer registers (16A-16D) storing various set values, and a buffer circuit (12) through which the count registers and the timer registers are coupled to said internal bus (18);
an incrementer (22) controlled by the operation controller (36) and coupled to the internal bus to

receive a value on the internal bus and coupled to a latch (24) to output either the received value incremented, if a count clock is active, or the received value without increment, if not so;
said latch (24) being controlled by the operation controller (36) to latch the value outputted from the incrementer (22) so as to output the latched value through the internal bus (18) to the buffer circuit (12),
the buffer circuit (12), the incrementer (22) and the latch (24) being controlled by the operation controller (36) so as to sequentially and cyclicly execute on the respective count registers in a time division manner such an operation that a value is read from one of the count registers to the internal bus (18) so as to be received by the incrementer (22), and the value outputted from the incrementer (22) is latched in the latch, and then, the value stored in the latch is written into the same count register, said operation respectively being executed on a count register in a corresponding count stage of a count cycle;
a coincidence flag (26) coupled to the register block (10) and having a plurality of outputs which correspond to the plurality of timer registers, respectively, and each of which supplies an output signal which is brought to an active level when the corresponding timer register detects a data coincidence, so that if the value to be written into a corresponding count register is coincident with the content previously set in the corresponding timer register, a corresponding one of the plurality of outputs of said coincidence flag (26) is brought to an active level by the corresponding timer register,
a clear controller (32) coupled to the coincidence flag so as to clear the count register having a count value in coincidence with the value of the corresponding timer register;

c h a r a c t e r i z e d in that each timer register (16A-16D) includes an array of content addressable memory cells so that each timer register has a comparison function for executing a coincidence detection between the value on the internal bus (18) to be written into a corresponding count register and the content previously set in the timer register itself, at each corresponding count stage of a count cycle in which the value on the internal bus (18) is to be written into a corresponding count register, said clear controller (32) clearing the latch in the corresponding count stage of the count cycle next to the count cycle in which the coincidence is detected, so that the cleared content of the latch is loaded and written into the corresponding count register."

After amendment, the description now cites documents D1 and D2 as relevant prior art and indicates that an object of the invention is a timer/counter for which the redesign of the whole circuit structure is not necessary when the number of count and timer registers is changed.

V. According to the appellant, the invention is not obvious since the type of memory used for the timer registers and the approach for clearing the count registers are substantially different from the prior art. Because of these differences, the mere idea to use a content addressable memory as timer register would not be sufficient to lead the skilled person to the inventive solution.

## Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

Present claim 1 is based on a combination of original claims 1 to 5 and 8. Further amendments, clarifying the function of the operation controller and the clear controller, are supported by the description as originally filed, in particular by page 11, first paragraph and page 12, second paragraph. Dependent claims 2 and 3 correspond to original claims 6 and 7, respectively. In addition to corrections of obvious mistakes, the description has only been amended to adapt the description to the claims and to indicate the relevant prior art. The amendments of description and claims do thus comply with the provisions of Article 123(2) EPC.

3. *Patentability*

3.1 Novelty

Document D1 is the only prior art document on file which discloses a timer/counter circuit comprising a register block of corresponding count and timer registers like in the present invention. The coincidence detection, however, is not a function of the timer registers themselves but of a separate comparing circuit connected via a common data line to the count registers and the timer registers, respectively. Accordingly, the reset mechanism for clearing of the count registers is also different. Furthermore, there is no hint given to use a content addressable memory (CAM) anywhere in this circuit.

Documents D2, D4, and D5 disclose timer/counter circuits without any memory locations corresponding to the timer registers of the present invention. In fact, they are not necessary since the count value is always counted up or down to the same final count value, namely either to a zero or an overflow value.

Document D3, finally, is directed to the design of CAM cells in MOS technology and remains silent as far as applications of those CAM cells are concerned.

The subject-matter of claim 1 has thus to be considered as novel (Article 54 EPC).

3.2 Inventive step

3.2.1 Closest prior art

A basic characteristic of the timer/counter circuit of the present invention is the register block comprising a plurality of corresponding count and timer registers. Only document D1 is directed to such a type of circuit and is thus considered as the closest prior art document.

3.2.2 Relevant difference

The subject-matter of present claim 1 differs from the circuit disclosed in document D1 primarily by the feature that each timer register has a comparison function for detecting coincidence events between count values and the preset timer value and by the particular mechanism for clearing the count registers as set out in the characterizing part of claim 1.

3.2.3 Problem solved

This difference does clearly not imply any improvement with regard to the performance of the circuit or the amount of chip area necessary to integrate the timer/counter circuit on a single chip. In particular with regard to the required chip area, a CAM generally requires a more complex internal structure than other types of memory so that its use does not lead per se to a reduction. The only advantage which can reasonably be expected to be achieved is an increased degree of modularity of the circuit by providing coincidence detection within each timer register, a solution which is based on the use of CAM cells as timer register and an appropriate circuit design for clearing the count registers. Therefore, the Board accepts that the subject-matter of claim 1, with respect to said closest prior art, solves the problem of simplifying the redesign when the number of count and timer registers is to be changed (see description, page 4a).

This problem, however, is also addressed by document D1 indicating that it might be advantageous or even necessary to change the number of storage locations and that for this reason the circuit design should allow for such changes in a simple and inexpensive way (see document D1, column 1 and column 8, second paragraph). The said problem of the present invention does thus not contribute to the inventive step.

3.3 Invention not obvious

None of the prior art documents on file, however, gives a hint to the circuit structure concerning the timer registers and to the reset mechanism for clearing the count registers of the present invention as defined in claim 1 for improving the modularity of the design, or even for any other reasons.

Document D2 illustrates in Figure 6 and describes, on page 5, a **high speed output subsystem** comprising a CAM for holding a compare value to be matched with the current content of a **Timer**. According to Figure 6, however, this match is done in a separate element designated in Figure 6 as **COMPARATOR**. The comparing function is thus not provided by the CAM itself but by this comparator like in the prior art of document D1, but contrary to the teaching of the present invention.

The other prior art documents D3, D4, and D5 are even less relevant than document D2. In view of the general technical knowledge, the examining division argued that the idea of using CAM cells in timer registers would be obvious to the skilled person. Indeed, the specific properties of a content addressable memory suggest several possible applications to the skilled person. For example, its associative function is suitable for providing a fast access to the individual cells of the memory, an important aspect if time is a critical parameter. However, the circuit design would have to be quite different from the structure of the register block 10 as defined in present claim 1. It is not difficult to find other similar examples so that this argument of the examining division does not hold with regard to the specific definition in claim 1.

4. For these reasons, the subject-matter of claim 1, and thus also the subject-matter of the dependent claims, is considered to involve an inventive step (Article 52(1) and 56 EPC). As with regard to the other requirements of the European patent convention the application does not cause any objections either, the main request can be allowed and there is no need to deal with the appellant's subsidiary request for oral proceedings.

## Order

**For these reasons it is decided that:**

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent in the version according to the main request.

The Registrar: The Chairman:

M. Beer P. K. J. van den Berg