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D E C I S I O N
of 10 January 1996

Case Number: T 0211/94 - 3.5.2

Application Number: 86116963.9

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Language of the proceedings: EN

Title of invention:
Protection circuit for a thyristor converter

Patentee:
KABUSHIKI KAISHA TOSHIBA

Opponent:
ASEA BROWN BOVERI AB

Headword:
-

Relevant legal provisions:
EPC Art. 56, 123(2)

Keyword:
"Added subject-matter - yes (main request)"
"Inventive step - no (auxiliary request)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0211/94 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 10 January 1996

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Decision under appeal: **Decision of the Opposition Division of the European Patent Office posted 7 January 1994 revoking European patent No. 0 225 618 pursuant to Article 102(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: R. G. O'Connell
C. Holtz

Summary of Facts and Submissions

I. The appellant contests the decision of the opposition division to revoke European patent No. 225 618. The reason given for the revocation was that the subject-matter of the claims then on file did not involve an inventive step, having regard to the following prior art:

D1: US-A-3 842 237
D2: DE-C-3 322 873.

II. In response to a written submission of the respondent the appellant filed new claims 1 to 4 on 26 April 1995.

III. Oral proceedings were held before the board on 10 January 1996 in the course of which the appellant submitted new claims 1 to 4 by way of a first auxiliary request and new claims 1 and 2 by way of a second auxiliary request.

IV. Claim 1 (main request) is now worded as follows:

"1. A protection circuit for a thyristor converter having a unit arm comprising a plurality of units connected in series, each unit including at least one thyristor, having

a plurality of forward voltage sense circuit means (41 - 4N) provided in the respective units, for sensing an application of a forward voltage, when the forward voltage is applied, each of the forward voltage sense circuit means (41 - 4N) sense that their corresponding unit is not in an ON state even though a forward voltage is applied,

first means (56) for detecting the time when the forward voltage is applied across the unit arm on the basis of output signals from the forward voltage sense circuit means and producing a detection output (co),

second means (55) for producing an operating signal (ca) when more than a predetermined number of the forward voltage sense circuit means have sensed that their corresponding unit is not in an ON state even though a forward voltage is applied,

third means (58, 62) for simultaneously delivering a protection gate firing instruction to all of the thyristors of the unit arm on the basis of both outputs from the first and second means being applied to the third means,

delay means (59) for delaying application of the detection output, wherein said

delay means (59) are provided between the first means (56) and a second input of the third means (58), the first input of the third means (58) being connected with the output of the second means (55, 57),

characterized in that

the forward voltage sense circuit means are adapted for continuously sensing the forward voltage across the unit arms and output a binary signal, and

the time delay is determined to delay the application of the detection output from the first means (56) to the third means (58) by a time required for compensating for variations in the operating characteristics of the forward voltage sense circuit means (41 - 4N)."

Claims 2 to 4 (main request) are dependent on claim 1.

Claim 1 (auxiliary request I) is worded as follows:

"1. A protection circuit for a thyristor converter having a unit arm comprising a plurality of units connected in series, each unit including at least one thyristor, having

a plurality of forward voltage sense circuit means (41 - 4N) provided in the respective units, for sensing an application of a forward voltage, when the forward voltage is applied, each of the forward voltage sense circuit means (41 - 4N) sense that their corresponding unit is not in an ON state even though a forward voltage is applied,

first means (56) for detecting the time when the forward voltage is applied across the unit arm on the basis of output signals from the forward voltage sense circuit means and producing a detection output (co),

second means (55) for producing an operating signal (ca) when more than a predetermined number of the forward voltage sense circuit means have sensed that their corresponding unit is not in an ON state even though a forward voltage is applied,

third means (58, 62) for simultaneously delivering a protection gate firing instruction to all of the thyristors of the unit arm on the basis of both outputs from the first and second means being applied to the third means,

delay means (59) for delaying application of the detection output, wherein

said delay means (59) are provided between the first means (56) and a second input of the third means (58), the first input of the third means (58) being connected with the output of the second means (55, 57),

characterized in that

signal converting circuits (9N - 91) are provided for outputting continuous binary signals (Pn - P1) based on the output signals of the forward voltage sense circuit means (4N - 41), said binary signals being input into the first and second means (56, 55), and

the time delay is determined to delay the application of the detection output from the first means (56) to the third means (58) by a time required for compensating for variations in the operating characteristics of the forward voltage sense circuit means (41 - 4N)."

Claims 2 to 4 (auxiliary request I) are dependent on claim 1.

Claim 1 (auxiliary request II) is worded as follows:

"1. A protection circuit for a thyristor converter having a unit arm comprising a plurality of units connected in series, each unit including at least one thyristor, having

a plurality of forward voltage sense circuit means (41 - 4N) provided in the respective units, for sensing an application of a forward voltage, when the forward voltage is applied, each of the forward voltage sense circuit means (41 - 4N) sense that their corresponding unit is not in an ON state even though a forward voltage is applied,

first means (56) for detecting the time when the forward voltage is applied across the unit arm on the basis of output signals from the forward voltage sense circuit means and producing a detection output (co),

second means (55) for producing an operating signal (ca) when more than a predetermined number of the forward voltage sense circuit means have sensed that their corresponding unit is not in an ON state even though a forward voltage is applied,

third means (58, 62) for simultaneously delivering a protection gate firing instruction to all of the thyristors of the unit arm on the basis of both outputs from the first and second means being applied to the third means,

delay means (59) for delaying application of the detection output, wherein

said delay means (59) are provided between the first means (56) and a second input of the third means (58), the first input of the third means (58) being connected with the output of the second means (55, 57),

characterized in that

signal converting circuits (9N - 91) are provided for outputting continuous binary signals (Pn - P1) based on the output signals of the forward voltage sense circuit means (4N - 41), said binary signals being input into the first and second means (56, 55),

said second means include an AND gate (55) for outputting the operating signal when all of the forward voltage sense circuit means (41 - 4N) sense that their corresponding units are not in an ON state even though a forward voltage is applied, and

the time delay is determined to delay the application of the detection output from the first means (56) to the third means (58) by a time required for compensating for variations in the operating characteristics of the forward voltage sense circuit means (41 - 4N)."

Claim 2 (auxiliary request II) is dependent on claim 1.

V. The appellant (proprietor) argued essentially as follows:

Main request

Article 123(2)

The first characterising feature of claim 1, viz "that the forward voltage sense circuit means are adapted for continuously sensing the forward voltage across the unit arms and output a binary signal", was derivable from a combination of Figures 1, 2 and 3 of the drawings as originally filed, in particular from a comparison of the waveform labelled "a" in Figures 2 and 3 with the waveforms P_n. An LED used to sense a voltage inherently generates a continuous signal; it was inconsistent to argue, as the opponent had done, that Figure 7 of D2 showed continuous sensing but that Figure 1 of the opposed patent, as interpreted by the waveform diagrams of Figures 2 and 3, did not.

Inventive step

D1, the closest prior art, did not teach continuous sensing of the blocking state of the thyristors; it employed a memory circuit 10 which latched incoming pulses for subsequent counting by element 5. As a result, the D1 circuit was incapable of detecting the important practical case in which a thyristor first recovers blocking ability, thus generating a pulse to be counted by unit 5 in the D1 circuit, then loses it again after a brief interval. The protection circuit as claimed in claim 1 (main request) solved this problem, which was not referred to in any prior art document, by monitoring continuous sensing signals dependent on the blocking conditions of the individual thyristors.

The appellant conceded that D2 (Figure 7) showed continuous sensing but argued that no plausible reason had been put forward as to why the skilled person should modify D1 in accordance with this particular detail of D2, nor why, starting from D2, this circuit, which does not have a time delay, should be adapted in accordance with the teaching of D1; this argument was an ex post facto mosaic.

As regards the second characterising feature - the criterion for determining the time delay - D1 did not suggest the claimed criterion; cf. D1, column 3, lines 59 to 68. In this respect claim 1 (main request) went beyond the prior art in identifying a criterion which could advantageously be used, in addition to other criteria, such as those specified in D1, in determining the optimum time delay.

The opponent's arguments in relation to very detailed timing relationships were not cogent; the time interval indicated at column 6, lines 50 to 56, of the patent in suit was an example for one embodiment and not a feature of the claim.

Auxiliary request I

Inventive step

Claim 1 of this request was not obviously derivable from D1 for the skilled person. D1 did not teach the use of continuous binary signals. In the latter document the pulse signals were counted in unit 5; there was no counting involved in the teaching of the opposed patent.

Auxiliary request II

Inventive step

The protection circuit as claimed in claim 1 of this request involving an AND gate for determining that all thyristors have recovered, in addition to the features already discussed, was particularly simple to implement and provided particularly strong protection against damage to thyristors. The prior art did not suggest this simple way of implementing a particular threshold value from the range of values taught by the prior art.

VI. The Respondents' arguments can be summarised as follows:

Main request

Article 123(2)

Neither "continuous sensing" nor its alleged advantage of taking account of short term recovery of a thyristor followed by renewed loss of blocking ability were disclosed in the application as originally filed. The signals P_n in Figures 2 and 3 of the patent were long term signals, but these signals were outputs of signal converter 9, which might have latching properties, just as the memory 10 in D1 had latching properties. The

alleged advantage over D1 which had been added to the description at column 4, lines 11 to 21, was not derivable from the original disclosure, even in the light of subsequently determined prior art such as D1. It was a spurious argument since the time delay referred to in the patent at column 6, line 54 of 10 to 100 microseconds would not allow time for an unstable recovery to be detected.

Inventive step

D1 showed a complex and sophisticated circuit involving a dynamically adapted time delay as its main embodiment, but it also disclosed at column 3, lines 56 ff, a "simple but less reliable" embodiment which used a fixed time delay as in the opposed patent. The skilled person would appreciate that such a simple fixed delay embodiment would not require the short term pulse signals required for the main complex embodiment and that long term binary signals would be preferable on grounds of circuit simplicity.

Auxiliary request I

Inventive step

The opponent contended that the protection circuit as claimed in claim 1 of this request was a functional equivalent for the skilled person of the simpler embodiment of D1 as mentioned at column 3, lines 56 to 64 of the latter document. This was evident when the memory unit 10 and the counter/threshold unit 5 of D1 were notionally enclosed in a box and viewed as a single functional unit.

Auxiliary request II

Inventive step

The protection circuit as claimed in claim 1 of this request represented an unrealistic and unnecessary borderline case. No inventive step was involved in lowering the threshold for protection firing to the case of a single thyristor failing to block, since such a criterion was technically devoid of merit; protection firing would then be so frequent that the circuit would hardly be usable in practice.

VII. The appellant requested, as main request, that the decision under appeal be set aside and that the patent be maintained, in amended form, on the basis of claims 1 to 4 as filed with letter dated 25 April 1995, received 26 April 1995 (main request). Alternatively, the appellant requested maintenance of the patent on the basis of claims 1 to 4 (auxiliary request I) submitted in the oral proceedings on 10 January 1996, or on the basis of claims 1 and 2 (auxiliary request II) submitted in the oral proceedings on 10 January 1996.

VIII. The respondent requested that the appeal be dismissed.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

Article 123(2)

2.1 The question to be decided under this heading is whether the feature "the forward voltage sensing circuit means are adapted for continuously sensing the forward voltage across the unit arms and output a binary signal" which was undisputedly not disclosed *expressis verbis* in the text of the description as originally filed, was nonetheless unambiguously derivable for the person skilled in the art from the waveform timing diagrams of Figures 2 and 3 in conjunction with the block diagram of the protection circuit shown in Figure 1.

2.2 In the board's judgement this feature is not unambiguously derivable from the illustration of the forward voltage sense circuit means (hereinafter FVSCM) designated 4N in Figure 1. This illustration is too schematic in nature to allow any definite conclusion about the kind of signal - pulse or continuous - output from the FVSCM proper, fed via light guide 7N and converted by corresponding light receiving element 8N and signal converting circuit 9N to a binary electric signal Pn (cf. page 7, lines 15 to 21,of the description of the application as originally filed). This conclusion is supported by a comparison with the similar schematic representation of the corresponding item (12) in Figure 1 of D1, which is explicitly described at column 2, lines 24 to 27 of D1 as "emitting an indicating pulse". Figs 2 and 3 of the application as originally filed do not provide any information about

the input signals to the signal converting circuit 9N. Since there is no mention of the feature in question in the text of the description and since the figures are consistent with either pulse or continuous input signals it must be concluded that the feature as specified in claim 1 is not directly and unambiguously derivable from the original disclosure. It follows that a patent including this claim would contain subject-matter which extends beyond the content of the application as filed thus contravening Article 123(2) EPC.

2.3 The appellant's main request is therefore not allowable.

3. *Auxiliary request I*

Article 123(2)

3.1 The specification in claim 1 of the second auxiliary request that "signal converting circuits are provided for outputting continuous binary signals based on the output signals of the forward voltage sense circuit means" overcomes the Article 123(2) objection which applied to claim 1 of the main request, since it is not disputed that the person skilled in the art would interpret the original description and drawings in this sense, in particular the waveforms for the signals P_1 to P_n in Figures 2 and 3 and the description of the operation of the combinational logic circuits 55 to 63 implies continuous binary signals at the outputs of the signal converting circuits 9N.

Inventive step

3.2 The opposed patent addresses the general problem of protecting a thyristor converter chain against partial turn-off, which occurs when the number of thyristors which recover a voltage blocking ability following

voltage reversal is so small that the individual recovered thyristors would be subject to a potentially destructive voltage; see column 1, lines 1 to 49 of the patent. The function of a protection circuit is to detect incipient partial turn-off and to deliver a protection gate firing instruction to all of the thyristors of the chain to forestall damage. Such a protection firing should ideally occur only when necessary, since it impairs the efficiency of the rectification operation. D1, the undisputed closest prior art, solves this problem by means of a circuit onto which the prior art portion of claim 1 of the amended patent (auxiliary request I) can be read if items referenced 4N, 55, 56, 58, and 59 of the claim are regarded as corresponding to items designated 1, 10+5, 3, 7, and 4 respectively of Fig 1 of D1. In particular, the D1 circuit includes a "second means" in the form of a memory circuit 10 with a threshold output element 5 (counter with output threshold) which detects the presence or absence of a number of recovered (i.e. blocking) thyristors exceeding a preset threshold number; a "delay means" in the form of an element 4 which develops a signal indicating that a predetermined time has elapsed since at least one thyristor recovered (D1, column 3, lines 56 to 59); and a "third means" in the form of an AND gate 7 for simultaneously delivering a protection gate firing signal to all thyristors of the unit arm on the basis of both outputs from the delay means (4) and from the "second means" (10+5) (D1, column 3, lines 26 to 32).

3.3 Relative to D1 the specific problem solved by the circuit according to claim 1 (auxiliary request I) is (i) to provide an alternative implementation of the circuitry for detecting that the number of recovered thyristors is above a predetermined number and (ii) to dimension the delay time of the delay means in

accordance with an alternative criterion, these problems being solved by modifying the prior art protection circuit in accordance with the first and second characterising features of the claim respectively.

3.4 Neither of these problems is regarded by the board as contributing in itself to inventive step since it is a matter of routine for the skilled person to consider alternatives of this kind.

3.5 As regards problem (i), the solution of latching or staticising the output signals of the forward voltage sense circuit means and feeding said staticised or continuous binary signals into the first means (for detecting the time when the forward voltage is applied across the unit arm on the basis of output signals from the forward voltage sense circuit means and producing a detection output) and the second means (for producing an operating signal when more than a predetermined number of the FVSCMSs have sensed that their corresponding unit is not in an ON state even though a forward voltage is applied, i.e. has recovered) amounts essentially to moving the latching or staticising stage which occurs at the input to the memory circuit 10 in D1 upstream to the point where the signals are received from the forward voltage sense circuit means.

3.6 In considering whether the skilled person would modify the D1 circuit in this way it has to be remembered that the main embodiment described and illustrated in D1 relates to a detection circuit involving a dynamic setting of the effective delay by a monostable element, whereas in the embodiment which represents the closest prior art a simple fixed delay element - as in the opposed patent - is proposed (D1, column 3, lines 56 to 64). A direct consequence of adopting this simpler implementation is that OR gate 3, corresponding to the

"first means" (for detecting the time when the forward voltage is applied across the unit arm on the basis of output signals from the forward voltage sense circuit means and producing a detection output) of the claim, need no longer pass on to element 4 the dynamic pulse signals from individual thyristor sense circuits but only a "first thyristor recovered" signal. Since staticised binary signals are preferred in circuit design when logic permits, a skilled person implementing the simpler version of D1 would, in the judgement of the board, at least consider as a circuit design option latching the signals at the detectors 2 (D1, Figure 1), corresponding to the "signal converting circuits" of the claim, and using these latched binary signals as a source for the units 3 and 10+5, corresponding to the "first and second means" of the claim. Circuit design considerations of this kind are part of the routine activity of the skilled person and do not involve an inventive step within the meaning of Article 56 EPC.

3.7 For the avoidance of doubt, it should be mentioned that the adoption of the measure specified as the second characterising feature in claim 1 (auxiliary request I) does not lead to the advantage over the closest prior art D1 referred to at column 4, lines 11 to 21 of the patent. This passage, which was added by way of prior art acknowledgement during the examination procedure, was based on an alleged advantage of the first characterising feature now specified in claim 1 of the main request, namely that continuous sensing of the sense circuit means would enable the "second means" to take account of a thyristor which first recovered a voltage blocking ability but then lost it again after a short interval. For the reasons indicated above the board has concluded that the latter feature represented an amendment which contravened Article 123(2). Since this alleged advantage would not necessarily be obtained

when the FVSCM signals are continuous binary signals after, but not necessarily before, the signal converting circuits as specified in claim 1 of the first auxiliary request, it cannot be relied on as evidence that the protection circuit of claim 1 of the first auxiliary request involves an inventive step.

3.8 Turning now to the second characterising feature of claim 1 of the first auxiliary request, that "the time delay is determined to delay the application of the detection output from the first means (56) to the third means (58) by a time required for compensating for variations in the operating characteristics of the forward voltage sense circuit means (41 - 4N)", it is noted that in D1 the criteria to be applied in setting the fixed delay t1 of the element 4, which corresponds to "the time delay" of the claim, are indicated as (i) (sufficiently long) that it may be assumed that a sufficient number of thyristors have time to recover during this period if they are faultless, but (ii) should possibly be made dependent on the working parameters of the thyristor rectifier, above all on the load. There is no explicit mention of compensation for variations in the operating characteristics of the FVSCM. However, the effects of the working parameters of the thyristors rectifier and the load are mediated in any protection circuit by the FVSCM so that, in the judgement of the board, it would be inconceivable that the skilled person would fail to take into account the variations in the operating characteristics of the latter in setting the time delay, at least to the extent of considering whether the variation was substantial enough to need taking account of. This is an application of the general principle that the characteristics of the measuring instrument are always liable to affect the result of a measurement. Although it cannot be excluded that an invention might be based on a discovery of a

hitherto unsuspected effect of a measuring instrument or sensing device, the board is not persuaded in the present case that the criterion mentioned in claim 1 should be regarded as anything other than a routine circuit design consideration for a person skilled in the art.

3.9 The appellant has not claimed, nor does the board discern any synergistic effect arising from the interaction of the two characterising features, so that the above piecemeal analysis is justified. The same applies to the relationship between the characterising features and the features of the prior art portion of the claim.

3.10 The board therefore concludes that claim 1 (auxiliary request I) does not involve an inventive step within the meaning of Article 56 EPC so that this request is not allowable.

4. *Auxiliary request II*

Article 123(2)

4.1 Independent claim 1 of this request effectively adds to claim 1 of the first auxiliary request the feature specified in claim 3 of the application as originally filed and of the patent as granted with the "logic circuit" being specified as an AND gate in accordance with the description and drawings as originally filed.

Inventive step

4.2 There are two additional features; (i) choosing the threshold for protection firing at the extreme level of requiring all thyristors to have recovered if such firing is not to occur and (ii) implementing this threshold by means of an AND gate.

4.3 As regards the first feature, the relevant problem relative to D1 is to select the threshold so as to minimise the probability that any thyristor of the chain would be subjected to a potentially destructive voltage and as regards the second feature the problem is to implement such a threshold in a simple way in circuit terms.

4.4 In the judgement of the board, the skilled person, in implementing the teaching of D1, would set the threshold corresponding to n_0 in D1 (D1, column 2, lines 51 to 64) at whatever level the circumstances required. In particular he would appreciate that the smaller the over-voltage margin of the individual thyristors the larger the number required to withstand safely the overall rectifier reverse voltage and the higher the value for n_0, up to the maximum logically possible value of setting n_0 equal to the total number of thyristors in the chain.

4.5 Neither does the board discern any inventive step in implementing this maximum threshold condition by means of an AND gate, this being a natural concomitant of the use of latched binary signals to record the blocking states of the respective thyristors (cf. point 3.6 above).

4.6 Hence, the board does not regard the subject-matter of claim 1 of auxiliary request II as involving an inventive step. This request is consequently not allowable.

5. *Other considerations*

The respondent also raised objections to the amended claims under Articles 57, 84 and 123(3) EPC. The board did not regard these objections as well-founded, but since they would not affect the outcome of the appeal their detailed consideration would be otiose.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

M. Kiehl

The Chairman:

W. J. L. Wheeler