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D E C I S I O N
of 28 April 1999

Case Number: T 0256/94 - 3.4.3

Application Number: 88119137.3

Publication Number: 0316912

IPC: H01L 23/48

Language of the proceedings: EN

Title of invention:
A bump electrode structure of a semiconductor device and a method for forming the same

Applicant:
Casio Computer Co., Ltd.

Opponent:
-

Headword:
Bump electrode structure/CASIO

Relevant legal provisions:
EPC Art. 123(2), 84, 54, 56

Keyword:
"Claims regarded as relevant source of disclosure"
"Amendments (allowable)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0256/94 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 28 April 1999

Appellant: Casio Computer Co., Ltd.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 19 November 1993 refusing European patent application No. 88 119 137.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
M. J. Vogel

Summary of Facts and Submissions

I. European patent application No. 88 119 137.3 was refused by a decision of the examining division dated 19 November 1993 on the ground that it did not comply with Article 123(2) EPC.

According to the decision, although individual features of claim 1 as amended were disclosed in the original application, they were taken out of their context and were generalized to an extent which went beyond the original disclosure. In particular, according to the decision, there was no basis in the original disclosure for the omission of the information about the material of the under-bump layer which was described in the application as combining a barrier function with a function to improve the bonding strength of the overlying bump, and thus had to be composed of an alloy of a barrier metal and a bonding metal.

Moreover, it was held in the decision that the original method claims 11 to 16 did not specify the materials forming the under-bump layer, and consequently, the claims did not define the invention in a complete and unambiguous manner. According to the decision, the content of claims 11 to 16 could not therefore be taken as a relevant source of disclosure.

II. The appellant (applicant) lodged an appeal on 19 January 1994 paying the appeal fee the same day, and filed a statement of the grounds of appeal on 23 March 1994 along with claims 1 to 7 and amended pages 1 to 3 of the description.

The appellant essentially contended that contrary to the opinion of the examining division, the original claims 11 to 16 achieved one of the objects of the invention stated in the application as filed, and therefore the claims were a relevant source for the subject matter of the amended claim 1. The appellant also submitted that claim 1 involved an inventive step having regard to the cited prior art.

III. In response to a communication from the Board, the appellant filed with its letter dated 13 November 1998, new claims 1 to 7 and an amended page 3 of the description, and requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: No. 1 to 7 filed with the letter of 13 November 1998

Description: Pages 4 to 10 as originally filed
Pages 1 and 2 filed with the statement of grounds
Page 3 filed with the letter of 13 November 1998

Drawings: Sheets 1/6 to 6/6 as originally filed

Furthermore, the appellant requested oral proceedings as an auxiliary request.

IV. Claim 1 of the above request reads as follows:

"A method for forming a bump electrode (16) of a semiconductor device so that the bump electrode (16)

protrudes from a central portion of the upper surface of the electrode pad (13) which is exposed through an opening (14a) of an insulating layer (14) and whose peripheral edge portion is covered by the insulating layer (14), said method comprising:

(a) a process for forming an under-bump layer (15) over the entire surface of the semiconductor device which has an electrode pad (13) exposed from the opening (14a) and an insulating layer (14) covering the periphery of the electrode pad (13);

(b) a process for forming a single photo-resist layer (19) on said under-bump layer (15) by dropping a wet photo-resist having a viscosity of hundreds of centipoises to approximately a thousand centipoises and spinning said semiconductor device;

(c) a process for etching an opening (19a) in the portion of said photo-resist layer (19) to a size such that the peripheral edge of said opening (19a) in said photo-resist layer (19) is situated between the respective peripheral edge portions of the opening (14a) of said insulating layer (14) and said electrode pad (13);

(d) a process for forming said bump electrode (16), including electro-plating through said portion of said photo-resist layer (19), so that the top surface of said bump electrode (16) is flush with or lower than that of said photo-resist layer (19); and

(e) a reactive-ion etching process for removing said under-bump layer (15) on said insulating layer (14) and simultaneously forming V-shaped grooves (17) on the surface of said bump electrode (16)."

V. Original claims 11, 15, and 16 read as follows:

"11. A method for forming a bump electrode (16) of a semiconductor device, characterized by comprising:

a process for forming an under-bump layer (15) over one entire face of the semiconductor device which has an electrode pad (13) and an insulating layer (14) covering the periphery of the electrode pad (13);

a process for forming the bump electrode (16) on that portion of the under-bump layer (15) facing said electrode pad (13); and

a reactive-ion (sputter) etching process for removing said under-bump layer (15) on the insulating layer (14) and forming fine V-shaped grooves (19) on the surface of the bump electrode (16)."

"15. The method of forming a bump electrode (16) of a semiconductor device according to claim 11, characterized in that said bump electrode (16) forming process includes steps of applying a wet resist to the surface of the under-bump layer (15), forming an opening (14a) in that portion of the wet resist facing the electrode pad (13) by etching, and forming the bump electrode (16) inside the opening by plating."

"16. The method of forming a bump electrode of a semiconductor device according to claim 15, characterized in that the outer peripheral edge of said opening (14a) is situated inside that of said electrode

pad (13), and said bump electrode (16) is thinner than the wet resist."

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments (Article 123(2) EPC)*

2.1 Claim 11 as filed seeks protection for a method for forming a bump electrode and contains features corresponding to features (a), (d) and (e) of the present claim 1, where the features in the latter claim are more specific than those in claim 11.

Claim 15 as filed is appended to claim 11 and includes features corresponding to features (b) and (c) of present claim 1, whereby the latter defines the formation of a photoresist layer, an opening in the photoresist layer and the formation of the bump electrode by plating in the opening in more specific terms than is the case in claim 15.

Originally filed claim 16 is appended to claim 15, which in turn is appended to claim 11, and includes features corresponding to features (c) and (d) of the present claim 1.

Thus original claim 16 seeks protection for a method including features corresponding to all the features (a) to (e) of present claim 1, the features (a) to (e) being more specific or narrower in

scope than those in claim 16.

2.2 Claim 1 is distinguished from the combination of originally filed claims 11, 15, and 16 in that:

(i) The preamble of claim 1 specifies that the resulting bump electrode protrudes from a central portion of the electrode pad and that electrode pad is exposed through an opening of an insulating layer, whereas claim 11 only states that the insulating layer covers the periphery of the electrode pad.

(ii) The viscosity of the photoresist in feature (b) is not specified in claims 11, 15, and 16.

(iii) The location of the peripheral edge portion in feature (c) is further specified to be between the respective peripheral edge portions of the opening of the insulating layer and the electrode pad. In original claim 16, the peripheral edge portion is only specified to be inside of the peripheral edge of the electrode pad.

(iv) In step (d), the process of forming the bump electrode "includes electro-plating" whereas claim 15 it is formed "by plating".

(v) Further, the top surface of the bump electrode is in step (d) specified to be "flush with or lower than" that of the photoresist, whereas original claim 16 only states that the bump is "thinner than" the wet resist.

2.3 The features (i) to (v) listed above have following basis in the application documents as originally filed (in the following, reference is made to the passages in the application as published):

(i) The basis for features (i) can be found in Figure 1 in conjunction with column 3, lines 19 to 36 and 47 to 55, as well as, the introductory portion of original claim 5.

(ii) The range of viscosity of the photoresist is given on column 4, lines 27 to 34.

(iii) The peripheral edge region is described in column 3, lines 47 to 50.

(iv) Electro-plating is mentioned in column 5, lines 7 to 10. The expression "including electro-plating" is based on the fact that in the embodiment described in the application, the bump 16 consists of two sub-layers 16a, 16b, where the upper sub-layer is formed by electro-plating and the lower sub-layer is formed using e.g. sputtering (cf. column 4, lines 21 to 25).

(v) The basis for "flush with" is found in column 5, lines 34 to 38 together with lines 10 to 14.

2.4 Thus, it follows from the above that all the features of the present claim 1 are *per se* disclosed in the originally filed application documents. In the decision under appeal, original claims 11 to 16 were not regarded as a relevant source of disclosure for the purpose of Article 123(2) EPC, since these claims did

not specify an essential feature of the invention, i.e. the composition of the under-bump layer. Moreover, the features in claim 1 were held by the examining division to be taken out of their original context and combined in a manner that was not originally disclosed.

2.4.1 It therefore has to be resolved first of all whether original claims 11 to 16 can be considered as a relevant source of disclosure for the present claim 1 or not.

The application as filed contained an independent claim 1 relating to a bump electrode structure, and independent claims 5 and 11 both relating to a method of forming a bump electrode. In the discussion of the prior art bump electrode with reference to Figure 5, it is stated in the application as filed, "The most important problem of the development is how to secure the bonding strength between the electrode pads and the under-bump layers, between the under-bump layer and the bump electrodes, and further **between the bump electrodes and the external lead terminals bonded thereto** when the top width (or diameter) of the bump electrodes is reduced" (see column 2, lines 3 to 10 of the published application; emphasis added by the Board). Two objects of the invention are stated in the application as filed, and in connection with the second object, it is stated in column 2, lines 17 to 21, "A second object of the invention is to provide a bump electrode structure of a semiconductor device which permits improved bonding strength per unit area of a bump electrode ...". In order to achieve this second object, according to the application as filed, "a bump electrode structure of a semiconductor device according

to the invention is constructed so that a bump electrode is bonded to an electrode pad with an under-bump layer therebetween, and fine V-shaped grooves are formed on the top surface of the bump electrode by anisotropic etching (see column 2, lines 39 to 45). An embodiment of the invention (and there is only one embodiment) to achieve the above object as well as the first object is described in the application as filed.

Claim 11 of the application as filed related to the solution of the second of the two stated objects of the invention, namely to provide a bump electrode structure of a semiconductor device which permits improved bonding strength per unit area of a bump electrode between the bump electrode and an external lead terminal (cf. column 2, lines 17 to 21 and 39 to 45), since it follows from the description that the V-shaped grooves formed on the bump electrode as set out in the claim provide a rough surface to which a solder (for bonding an external lead terminal) would anchor with high reliability (see column 7, lines 12 to 16). Original claims 1 to 10 on the other hand were directed to the first object which related to a bump electrode structure capable of being bonded to a fine electrode pad with sufficient strength and reliability (cf. column 2, lines 11 to 39), and it was evident from the application as filed that the dual functions of the under-bump layer acting as a barrier layer and a bonding layer were essential only for attaining the first object (cf. column 3, lines 39 to 42).

Thus, contrary to the finding of the examining division, in the Board's view, there was no inconsistency between the invention as defined in

original claim 11 and the general statement of one of the objects of the invention in the description. Under these circumstances, the subject matter of claim 11 clearly formed part of the content of the application as filed, and consequently, has to be taken into consideration for the purpose of Article 123(2) EPC.

Also, in the Board's view, even if an application as filed contained an independent claim which did not achieve the only stated object of the invention, the subject matter of the claim cannot be disregarded for the purpose of Article 123(2) EPC simply because the claim did not contain all the features essential to achieving the stated object. This is because, in the consideration of the requirements of Article 123(2) EPC, it is the total information content of the application at the filing date, including the subject matter of an independent claim defining the invention, which has to be taken into account. Any inconsistency between the invention as defined in the claim and as described can be resolved by amending the description or the claim as appropriate, during the subsequent examination pursuant to Article 96(2) EPC without contravening Article 123(2) EPC.

2.4.2 A further question which needs to be answered is whether features (i) to (v) are taken out of their original context and combined with the features of claim 16, in a manner such that such a combination, as in present claim 1, generates a new invention extending beyond the content of the application as filed.

As already stated under point 2.4.1 above, the application as filed sought protection, inter alia, for

a method as defined in original claim 16 including the features of original claims 15 and 11. Moreover, it follows from the statements in column 2, lines 46 to 49 and column 3, lines 16 to 18 of the published application that first, second and other objects and **features of the invention** are described in detail in the only embodiment of the invention. As stated under point 2.3 above, features (i) to (v) are all disclosed in the only embodiment of the invention, so that their combination as in the present claim 1 does not provide any further information about the invention which was not in the application as filed.

In connection with the above, the Board also notes that the specific structure of the electrode as set out in feature (i) above and the formation of the photoresist layer by spinning using the specified viscosity values as in feature (ii) are disclosed in original claims 5 and 8 only in combination with an under-bump layer formed of an alloy of a barrier metal and a bonding metal, and a photoresist layer having a thickness of 20 to 30 µm. However, the Board sees no technical reasons in the description of the specific embodiment why the composition of the under-bump layer was essential to the solution of the problem addressed by the present claim 1 or why the viscosity values as specified in the claim were to be employed **only** for a photoresist layer having a thickness in the range of 20 to 30 µm. Thus, the features (i) and (ii) are not taken out of context.

3. For the foregoing reasons, in the Board's judgment, claim 1 as amended complies with the requirements of Article 123(2) EPC.

The description has been amended for consistency with the amended claim 1. The application as amended therefore does not contravene Article 123(2) EPC.

4. *Clarity (Article 84 EPC)*

There is no objection against the amended claim 1 under Article 84 EPC. In particular the essential features for achieving the object of the invention as stated in the amended description on page 2, lines 31 to 34. The amended description on page 2, lines 27 to 30 refers only to improving bonding strength between the bump electrode and an external lead.

5. *Novelty and inventive step (Article 52(1) EPC)*

5.1 Document D1 discloses formation of a bump electrode (28) on a portion of a bonding pad (26) exposed through an opening (34) in an insulating layer (30) (cf. Figure 4; column 2, line 58 to column 3, line 6). An under-bump layer as in step (a) of the present claim 1 is however not provided, and, consequently, an etching step to remove as in step (e) is also not required in the process of document D1. Also, the problem of improving the bonding strength of a lead terminal is not addressed in this document.

5.2 Document D2 discloses a mushroom shaped bump electrode (see Figure 1) in connection with a TAB assembly (see page 773, III TAB PROCESS FLOW). The method disclosed comprised the formation of an under-bump layer as in step (a), formation of a wet resist having a thickness so as to avoid "mushrooming" of the bump electrode (page 773, right-hand column, second paragraph),

alignment of the opening in the photoresist so that the bump electrode formed by plating extends over the edge of the opening in the insulating layer (page 773, right-hand column, third paragraph) as in step (c), wet etching of the bump electrode of gold and subsequently wet etching or plasma etching to strip the under-bump layer (page 774, left-hand column, second paragraph).

The plasma etching to remove the under-bump layer is not disclosed to be RIE type, i.e. anisotropic. In the Board's view on the contrary, since the plasma-etching is employed to strip the exposed under-bump layer, the plasma-etching has to be isotropic. Moreover, a KI solution, i.e. a wet etching, is exclusively advised to be used for the gold removal. The teaching of D2 therefore indicates that a plasma etch would not be suitable for structuring the gold surface. Consequently, there is no disclosure that such plasma etching would produce V-shaped grooves on the upper surface of the bump electrode as in step (e). Moreover, document D2 also does not deal with the problem of adhesion of a lead terminal to the bump-electrode.

5.3 Document D3 describes a process of forming a bump electrode on an under-bump layer (cf. page 72, "Current Honeywell Bumping Technology", pages 72 to 74; Figures 5 and 6). The use of RIE etching as in step (e) of claim 1 is not disclosed, since the under-bump layer in the method of D3 is removed by wet etching (cf. page 74, left-hand column, fourth paragraph). Document D3 is also not concerned with improving the bonding strength between the bump electrode and a terminal lead.

5.4 Thus, the subject matter of claim 1 is new within the meaning of Article 54 EPC.

5.5 In relation to document D2, which the Board considers to be the closest available prior art, the problem which the present application seeks to solve can be regarded as improving the bonding strength between the bump electrode and a lead terminal. Documents D1 to D3 neither address this problem nor suggest the step of RIE etching to remove the under-bump layer and simultaneously to provide V-shaped grooves as in step (e) of claim 1. The claimed method is therefore not rendered obvious by the cited prior art.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the following documents:

Claims: No. 1 to 7 filed with the letter of 13 November 1998;

Description: Pages 4 to 10 as originally filed;
Pages 1 and 2 filed with the statement of grounds;
Page 3 filed with the letter of 13 November 1998;

Drawings: Sheets 1/6 to 6/6 as originally filed.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla