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D E C I S I O N
of 14 March 1997

Case Number: T 0283/94 - 3.4.1

Application Number: 88120975.3

Publication Number: 0321860

IPC: H01L 21/82

Language of the proceedings: EN

Title of invention:
Process for manufacturing integrated capacitors in mos technology

Applicant:
SGS-THOMSON MICROELECTRONICS S.r.l.

Opponent:
-

Headword:
Integrated capacitors/SGS-THOMSON MICROELECTRONICS

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"
"Contingent request for the extension of the appeal proceedings for 10 days, submitted during the oral proceedings - denied"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0283/94 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 14 March 1997

Appellant: SGS-THOMSON MICROELECTRONICS S.r.l.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 19 November 1993 refusing European patent application No. 88 120 975.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. D. Paterson
Members: R. K. Shukla
Y. J. F. Van Henden

Summary of Facts and Submissions

I. European patent application No. 88 120 975.3 claiming the priority date of 23 December, 1987 was refused by a decision of the Examining Division on the grounds that the application did not meet the requirements of novelty and inventive step pursuant to Articles 52(1), 54(1) and (2), and 56 EPC having regard to the prior art documents,

D1: US-A- 4 577 390,
D2: Journal of Vacuum Science Technology, B5 (6), Nov/Dec 1987, pages 1555 to 1563, and
D3: WO-A- 8 100 171.

II. Documents D1 and D2 had been listed in the European search report.

During the proceedings before the Examining Division, in its first communication dated 29 May 1992 the above documents D1, D2 and D3 were relied upon as indicating lack of novelty and inventive step in all the claims on file. In a reply dated 23 October 1992 the applicant filed amended claims in order to meet the objections raised, and submitted that such amended claims were both novel and inventive over the disclosures of documents D1 and D2. The publication date of document D2 before the priority date of the application was not challenged. In a further communication dated 7 May 1993 annexed to a summons to oral proceedings, the Examining Division continued to rely upon documents D1 and D2 against the amended set of claims; and following cancellation of the oral proceedings the Examining Division issued its decision refusing the application on the ground of lack of novelty and inventive step of the claimed invention, having regard to documents D1 and D2.

III. The Applicant lodged an appeal against the above decision and requested the grant of a patent based on an amended set of claims 1 to 4 as the main request; the only independent claim 1 of the set has the following wording:

"Process for manufacturing integrated capacitors in MOS technology on a substrate already bearing doping implantations, comprising the steps of:

producing, in said substrate (1) of semiconductor material, having a first type of conductivity, a first layer (6) of conducting material to form a first plate,

providing a layer (7) of dielectric material at least partially superimposed and in contact with said first layer (6) of conducting material, and

providing a second layer (8) of conducting material superimposed and in contact with said layer (7) of dielectric material, to form the second plate of the capacitor,

characterised in that

the provision of said layer (7) of dielectric material is constituted by a step of depositing a single layer of silicon oxide at a selected low temperature, said selected low temperature being in the range of the temperatures not affecting the displacement of doping implantations.

IV. In a communication annexed to a summons to oral proceedings, the Board informed the Applicant of its provisional view that although the subject-matter of amended claim 1 was new in relation to document D1, it apparently lacked an inventive step having regard to documents D3 and D2.

The communication stated that "Any submissions or requests should be filed at least one month before the date of the oral proceedings. Late filed submissions or requests may be admitted into the proceedings only at the discretion of the Board under exceptional circumstances."

V. In its response dated 12 February 1997 to the above communication, the Applicant made submissions in support of inventive step having regard to documents D3 and D2.

VI. Oral proceedings were held on 14 March 1997. At the commencement of the oral proceedings, the Applicant pointed out that on document D2 only "Nov/Dec 1987" is printed as the period of its publication, so that it is not clear whether or not this document was made available to the public before the priority date (23 December, 1987) of the application in suit. The Applicant therefore requested that in the event that the Board was to consider that the invention as claimed lacks an inventive step having regard to this document, then the oral proceedings be terminated without a decision and that the Applicant be a given a time limit of about ten days to ascertain whether or not the document is comprised in the state of the art according to Article 54(2) EPC.

An auxiliary request based on a further amended claim 1 was filed at the oral proceedings. In relation to claim 1 of the main request as set out in paragraph III above, claim 1 of the auxiliary request contains the following amendments:

(i) insertion of "thin" between "a single" and "layer" and
(ii) insertion of "such that the capacitors defined by said layers have a low voltage coefficient".

The Applicant also expressed his willingness to amend the feature (ii) above further, whereby the feature (ii) as further amended would read, "such that the capacitors defined by said layers have a maximum voltage coefficient of approximately 20 ppm/volt", if such an amendment would overcome the objection of lack of inventive step.

VII. The Applicant made essentially the following submissions in support of an inventive step in the subject-matter as claimed in claims 1 of the main and auxiliary requests respectively :

It is evident from Table I in document D2 that although the low temperature oxidation processes such as TEOS-SiO2 and LTO are free from out-diffusion problems, thin films obtained by these processes do not possess good electrical characteristics. Moreover, in section VI "Conclusion ", the authors of the article recommend the use of HTO process involving relatively high temperature, as against low-temperature oxidation processes such as TEOS and LTO, to provide very thin films of "gate- oxide quality". It also follows from the abstract of the document that in the TEOS process the films are not uniform in thickness across the wafers to a degree required in analog capacitors. Finally, whereas in the process according to document

D3, oxygen environment is used, document D2 explicitly recommends that the process be carried out without oxygen so that the film uniformity is not impaired. To a skilled person concerned with providing a dielectric film of a low voltage coefficient, i.e. a voltage coefficient not exceeding 20 ppm/volt, in a capacitor of a precision analog circuit as in the present application, the disclosure in document D2 does not provide any incentive to use TEOS or LTO oxidation processes in the method disclosed in document D3. On the contrary, the teaching of document D2 would lead him away from such a use.

VIII. After hearing the submissions made by the Applicant in relation to inventive step having regard to documents D3 and D2, the Board announced the decision that the appeal is dismissed.

IX. Following such oral proceedings on 14 March 1997, the Applicant filed a letter on 18 March 1997 enclosing a copy of document D2 marked with a date of receipt of 8 January 1988 at the German Patent Office.

Reasons for the Decision

1. *Procedural matters*

The file record of the present application as summarised in paragraph II above shows that throughout the examination proceedings document D2 was relied upon by the Examining Division as a prior art document according to Article 54(2) EPC, relevant to the issue of inventive step.

Furthermore, as can be seen from paragraphs IV, V and VI above, although document D2 was accepted by the Applicant as a prior art document relevant to the issue of inventive step during the written stage of the present appeal proceedings, the Applicant raised a question concerning the publication date of document D2 for the first time during the oral proceedings before the Board of Appeal.

In the Board's view, a document having a "nominal publication date" (i.e. a printed date on it, or range of dates, such as document D2 in the present case) before (or, for a range of dates, primarily before) the priority date, can prima facie be regarded as belonging to the state of the art according to Article 54(2), and can accordingly be relied upon as being part of the art during examination proceedings pursuant to Article 96(2) EPC, unless and until the Applicant credibly challenges the actual publication date as not being before the relevant priority date, during such examination proceedings. It can be normally expected that an Applicant who wishes to challenge the actual publication date as not being before the priority date will do so in reply to the first communication under Article 96(2) EPC in which the document is relied upon as a prior publication: because a European patent attorney can normally be expected to check whether a document which is relied upon during examination proceedings as having been made available to the public in accordance with Article 54(2) EPC was in fact a prior publication at the relevant priority date, as soon as such document is cited - this being part of the professional duty of a patent attorney.

In the present case the Applicant did not challenge the publication date of document D2 throughout the examination and appeal proceedings, during nearly five years following the first communication under

Article 96(2) EPC, until the oral proceedings before the Board of Appeal. During the whole of this period the Applicant on the contrary accepted that document D2 was within the state of the art. Furthermore, even at the oral proceedings the applicant did not credibly challenge the publication date (for example by credible evidence), but merely requested an adjournment of ten days during which some investigations would be carried out, apparently for the first time. This was in spite of the clear statement in the Board's communication accompanying the summons to oral proceedings, which is quoted in paragraph IV above.

In the above circumstances, the Board decided to exercise its discretion by not allowing more time for investigation of the publication date of document D2, and accordingly announced its decision to dismiss the appeal at the end of oral proceedings on 14 March 1997. Consequently, the letter filed on 18 March 1997 cannot be admitted into the proceedings, which were terminated by announcement of the decision on 14 March 1997.

2. *Inventive step*

The only issue which remains to be considered is, therefore, that of inventive step. In the following, this issue is discussed in relation to the subject-matter of claim 1 of the auxiliary request (see paragraph VI, second sub-paragraph); the following findings against the patentability are therefore applicable to claim 1 according to the main request.

2.1 The prior art coming closest to the claimed invention is disclosed in document D3, which describes a process for manufacturing integrated capacitors in MOS technology as set out in the precharacterising part of the claim (see pages 4 and 5 and Figures 1 to 4). Also,

in the present application as published (see column 2, lines 15 to 32) it is acknowledged that such a process is known in the art.

Moreover, as shown in Figure 3 and described on page 5, second paragraph of document D3, the capacitor dielectric (30) is constituted by a thin single layer of silicon dioxide formed by heating the entire chip in an ambience of oxygen to a temperature of around 1070°C.

The process according to claim 1 of the auxiliary request is thus distinguished over the process known from Document D3 in that the silicon oxide is formed at a low temperature at which there is no displacement of the implanted impurities and in that the capacitor defined by said layers has a low voltage coefficient.

2.2 The objective technical problem underlying the present invention is set out in column 3, lines 2 to 12 and column 1, lines 21 to 28 of the published application, i.e. to provide a process for manufacturing capacitors having electrical characteristics which comply with the requirements such as small size, precise capacitance value, low current loss, and most importantly low voltage coefficient, and which at the same time do not affect other components of the device in which they are integrated by setting lower limits to the minimum obtainable dimensions.

2.3 Document D2 describes deposition of high quality thin (49 nm thick) SiO2 film by pyrolysis of tetraethylorthosilicate at temperatures between 650 and 800°C. In Table I on page 1556 where properties of the TEOS-SiO_2 film are summarised, it is stated that the low deposition temperatures employed in the process avoids out-diffusion problems. For a detailed evaluation of electrical properties of the low temperature film, reference is made at the bottom of the Table to Section

V entitled, "Electrical Characterisation" where electrical properties such as dielectric breakdown strength, C-V hysteresis, interface densities etc. of the film are discussed in detail, and in Section VI "Conclusion", it is stated that the TEOS-SiO_2 films show an excellent step coverage, and a good uniformity, enable the preservation of shallow junctions, and do not require an additional high temperature step for densification of the film (see the first paragraph). It is further concluded that the TEOS-SiO_2 films show a high dielectric breakdown strength (8 $MVcm^{-1}$), a low failure rate after current stress and no hysteresis in C-V scans (see the third paragraph). Although the interface state densities are stated to be slightly higher than those of thermal oxides, page 1561, right-hand column, first paragraph discloses that since the interface density (of the TEOS-SiO2) is not higher than 10^{10} $eV^{-1}cm^{-2}$, it is not limiting for use of the film in VLSI circuits.

The Board agrees with the Applicant's submission that where the deposition of very thin films of "gate-oxide" quality is required, the authors of document D2 recommend the use of the HTO process involving relatively high temperature as against the use of the low-temperature oxidation process such as TEOS or LTO. However, this statement applies to ***very thin*** films of "gate-oxide" quality, and secondly it merely ***recommends*** the use of the HTO process under these circumstances. Moreover, this isolated statement has to be balanced against the beneficial electrical properties of the TEOS film discussed above and more importantly against the fact that the TEOS process avoids out-diffusion of dopants, so that it cannot be realistically concluded from the above statement that the skilled person would not even contemplate the use of the TEOS process in the process of document D3. On the contrary, under the

circumstances of the present case where the deposition process is to be optimised taking into account somewhat conflicting requirements, i.e. prevention of out-diffusion by using a relatively low temperature deposition process on the one hand and good electrical properties, in particular a low voltage coefficient, required for a capacitor on the other hand, in the Board's view, the skilled person would at least be led to try the TEOS deposition process in the process according to document D3 with a view to avoiding out - diffusion. Such routine trials would inevitably provide capacitor dielectrics having the required low voltage coefficient not greater than 20 ppm/volt.

2.4 For the foregoing reasons, in the Board's judgment the subject-matter of claim 1 forming the basis of the main and auxiliary requests was obvious to the skilled person having regard to documents D2 and D3.

2.5 The unformulated further request of the Applicant which is referred to in the final sub-paragraph of paragraph VI above was also obvious for the foregoing reasons.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer G. D. Paterson