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D E C I S I O N
of 30 May 1996

Case Number: T 0410/94 - 3.4.1

Application Number: 84300212.2

Publication Number: 0117045

IPC: H01L 27/02

Language of the proceedings: EN

Title of invention:
liquid crystal flat panel display

Patentee:
OIS Optical Imaging Systems, Inc.

Opponent:
Philips Electronics N.V.

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes)"
"Unallowable ex post facto interpretation of a prior art document"

Decisions cited:
-

Catchword:
-

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Case Number: T 0410/94 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 30 May 1996

Appellant: (Opponent)
Philips Electronics N.V.
Groenewoudseweg 1
NL-5621 BA Eindhoven (NL)

Representative:
Raap, Adriaan Yde
INTERNATIONAAL OCTROOIBUREAU B.V.
Prof. Holstlaan 6
5656 AA Eindhoven (NL)

Respondent: (Proprietor of the patent)
OIS Optical Imaging Systems, Inc.
1896 Barrett Street
Troy
Michigan 48084 (US)

Representative:
Müller, Hans-Jürgen, Dipl.-Ing.
Müller, Schupfner & Gauger
Postfach 10 11 61
80085 München (DE)

Decision under appeal: **Decision of the Opposition Division of the European Patent Office dated 21 February 1994 rejecting the opposition filed against European patent No. 0 117 045 pursuant to Article 102(2) EPC.**

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Composition of the Board:

Chairman: G. D. Paterson
Members: H. J. Reich
R. K. Shukla

Summary of Facts and Submissions

I. The Respondent is the proprietor of European patent No. 0 117 045.

Claim 1 as granted reads as follows:

"1. Flat panel display comprising: at least one pixel (70), said pixel including three address leads (72, 74, 80); first and second diodes (84, 86) connected together, with the cathode of said first diode (86) electrically connected to the anode of said second diode (84), said diodes (84, 86) being connected between two of said address leads (74, 80), with the anode of said first diode connected to a first address lead (80) and the cathode of said second diode (84) connected to a second address lead (74); each of said diodes (84, 86) being formed of a first layer (40a) of doped amorphous silicon alloy material, a layer (40b) of intrinsic amorphous silicon alloy material overlying said first doped layer (40a), and a second doped layer (40c) of amorphous silicon alloy material overlying said intrinsic layer (40b); said first and second doped amorphous silicon layers (40a, 40c) being opposite in conductivity type; a first conductive electrode (94) electrically connected to the cathode of said first diode (86); and to the anode of said second diode (84); a second conductive electrode (96) spaced with respect to said first electrode (94); said second electrode electrically connected to the third address lead (72); and liquid crystal material disposed between said electrodes (94, 96)."

Granted Claims 2 to 5 are dependent on Claim 1.

II. This patent was opposed by the Appellant on the grounds mentioned in Article 100(a) EPC, in particular Article 56 EPC having regard to documents:

D4: US-A-4 217 374;

D5: Proceedings of the IEEE, vol. 59, No. 11, November 1971, pages 1566 to 1579;

D6: Journal of Applied Physics, vol. 51, No. 8, 1980, pages 4287 to 4290; and

D7: US-A-4 223 308.

III. The Opposition Division rejected the opposition for the following reasons:

The subject-matter of Claim 1 differs from the closest prior art disclosed in document D5 in that the pixels of the flat panel display as claimed comprise amorphous silicon p-i-n diodes. Within the disclosure of document D5 a skilled person having the objective of reducing the process steps, would find no incentive to use a-Si p-i-n diodes in the D^2C addressed liquid crystal display (LCD) according to Figure 19 of document D5. Such a use seems not to be obvious, since no available document published in between the publication of document D5 in 1971 and the priority year of the invention in 1983 describes LCDs with a-Si p-i-n diodes, although p-i-n diodes made of crystalline material were already known in the art. Document D6 provides a hint to a skilled person to use a-Si p-i-n diodes only in solar cells, whereas for LCDs a-Si p-n diodes are recommended, in particular with very low doped p-n junctions for obtaining low reverse leakage currents. Curve a' in Figure 3 of document D6 seems to represent the lower limit of a set of curves

corresponding to p-n diodes and not a curve corresponding to a p-i-n diode. No explicit reference to p-i-n diode characteristics could be found in document D6.

IV. The Opponent lodged an appeal against this decision and cited in the grounds of appeal four new documents:

D8: Thin Solid Films, vol. 90, 1982, pages 359 to 370;

D9: IBM Technical Disclosure Bulletin, vol. 16, No. 10, March 1974; pages 3402 to 3404;

D10: DE-A-3 119 481;

D11: S. M. Sze: "Physics of Seimiconductor Devices, Second Edition, John Wiley & Sons, New York, 1981, pages 117 to 122.

V. In a communication accompanying a summons to oral proceedings the Board informed the parties of its provisional view that document D9 in combination with document D6 might possibly be decisive for the decision to be taken and therefore document D9 might be considered by the Board under Article 114(1) EPC.

VI. Oral proceedings were duly held on 30 May 1996. The Opponent requested that the decision under appeal be set aside and that European patent No. 0 117 045 be revoked. The Patentee requested that the appeal be dismissed and that the patent be maintained as granted.

VII. In support of its request the Opponent argued essentially as follows:

(a) Document D9 comes closer to the subject-matter of Claim 1 than document D5 since no capacitor needs

to be provided parallel to the liquid crystal cell for increasing its brightness. Moreover, document D9 specifies a list of indispensable diode properties, among them the most stringent demand of low reverse leakage current. Hence, document D9 gives a skilled person a clear incentive to look for a diode with a low reverse leakage current.

(b) Document D9 states that the semiconductor film comprising the diodes "**may** consist of polycrystalline material". Such statement does not exclude the use of amorphous material, since there is no sharp boundary between polycrystalline and amorphous material. Accordingly, the description of the opposed patent, column 7, paragraph 1 defines the term "amorphous" as a material which "contains at times crystalline inclusions". Furthermore, document D6, page 4287, left-column, paragraph 1 shows that the use of amorphous silicon p-n diodes was known in the addressing of large area LCDs wherein two diodes were placed back-to-back in series with each pixel. Using amorphous silicon for realising the claimed three-terminal arrangement would therefore be obvious.

(c) Document D6 discloses the forward and reverse current-voltage characteristics of amorphous silicon diodes having a p^+-p-n-n^+ structure, as a function of the doping level of the p and n layers. Figure 3 of document D6 shows that the reverse leakage current decreases with decreasing p and n concentrations between the p^+ and n^+ regions, the lowest reverse leakage current having been found for $p = 0.03 \cdot 10^{-3}$ and $n = 0$ (curve a'). The doping density $n = 0$ means, that the n region of the p^+-p-n-n^+ structure is intrinsic so that curve a' will be understood as the reverse leakage current

characteristics of an amorphous silicon p-i-n diode. The last sentence of the abstract of document D6 teaches explicitly to use these diodes in matrix-addressed large-area LCDs. All further properties of a p-i-n structure are generally known as can be seen from document D11.

(d) Since no surprising effects of the p-i-n structure can be derived from the disclosure of the opposed patent, the subject-matter of Claim 1 represents an obvious choice of the a-Si p-i-n diode disclosed in document D6 in the flat panel display scheme disclosed in document D9.

VIII. The above arguments were contested by the Patentee, who made essentially the following submissions:

(a) The objective of the present invention is to satisfy the long felt need of a very cheap mass-produced large screen flat panel display with high resolution, i.e. high packing density, wherein the same pixel properties can be realised with high tolerance of the production parameters. This objective is achieved in an unexpected way by starting from the three-terminal device disclosed in document D9 and replacing the polycrystalline silicon material and the pn-junction diode used in document D9 by amorphous silicon material and a p-i-n diode. This replacement surprisingly results in uniform panel characteristics with good gray scale performance.

(b) Document D9 comes nearer to the invention than document D5 considered by the Opposition Division. The criterion of low reverse leakage current for a diode, mentioned in document D9, is generally known to be advantageous for any circuit, and is not

restricted to address circuits of liquid crystal displays. Address circuits for liquid crystal cells wherein no capacitors are provided parallel to each cell unit represent a conventional device structure which was known before the publication date of document D5 in 1971. Document D5 concerns a particular further development of the conventional cell arrangement without capacitors and teaches to add a capacitor parallel to each cell in order to increase the brightness of the display.

(c) Document D6, page 4287, left column, paragraph 1 summarises the technical background of the investigation described in document D6 and shows that the use of a-Si p-i-n diodes was restricted to solar-cells, whereas large area liquid crystal displays were addressed by two back to back a-Si **p-n junction** diodes. A skilled person derives from document D6 exclusively the forward and reverse current-voltage characteristics of a p-n junction diode for various doping levels of the n and p regions of the p-n junction, measured in a p^+-p-n-n^+ structure. Since the p^+ and n^+ regions are extremely narrow, they form terminals with low contact resistance to the investigated p and n regions and are thus not part of the regions forming the diode itself. Curve a' in Figure 3 of document D6 demonstrates the results for the limit of the doping density n = 0 of the stepwise lowered doping densities of the p-n junction diode. A skilled person would not conclude from the disclosure of document D6 that the incidental intrinsic property of the n-part of the p-n junction converts this investigated structure into a p-i-n diode. Such an interpretation would be based on hindsight. There is no hint derivable from document D6 to use an a-Si p-i-n diode for addressing a liquid crystal

display, in particular to use such diode in a three-terminal device. Document D6, page 4289, right column, paragraph 4 teaches that the properties of diodes made of amorphous silicon, are not fully understood, even for a p-n junction. This fact illustrates that at the priority date of the present invention a skilled person was not able to predict any diode properties of a p-i-n structure realised in amorphous silicon. The invention was based on a fortuitous discovery and is thus not obvious.

IX. At the conclusion of the oral proceedings the decision was announced that the appeal is dismissed.

Reasons for the Decision

1. The Board considers that late-filed document D8, D10 and D11 cited for the first time in the Grounds of Appeal have no influence on the decision to be taken, so that these documents are disregarded under Article 114(2) EPC. It is apparent from paragraphs VII and VIII above that document D9 was fully considered by both parties during the oral proceedings before the Board, and this document is accordingly admitted into the appeal proceedings pursuant to Article 114 EPC.

2. *Inventive step - Claim 1*

2.1 The only substantive issue raised in this appeal is that of inventive step.

2.2 Having regard to the features defined by the wording of Claim 1, it makes no difference whether the disclosure of document D5 or that of document D9 is regarded as

forming the closest prior art. A skilled person derives from Figure 19 of document D5 as well as from Figure 1 of document D9 the following features of Claim 1:

"Flat panel display comprising: at least one pixel said pixel including three address leads; first and second diodes connected together, with the cathode of said first diode electrically connected to the anode of said second diode, said diodes being connected between two of said address leads, with the anode of said first diode connected to a first address lead and the cathode a said second diode connected to a second address lead; a first conductive electrode electrically connected to the cathode of said first diode and to the anode of said second diode; a second conductive electrode spaced with respect to said first electrode; said second electrode electrically connected to the third address lead; and liquid crystal material disposed between said electrodes"

However, in view of the Opponent's submission in paragraph VII above, the subsequent examination of inventive step can be limited to the question whether it was obvious to a skilled person to replace in the flat panel display disclosed in document D9, the p-n junction diodes made of polycrystalline silicon by a-Si p-i-n diodes corresponding to the remaining wording of Claim 1, i.e.

"each of said diodes being formed of a first layer of doped amorphous silicon alloy material, a layer of intrinsic amorphous silicon alloy material overlying said first doped layer, and a second doped layer of amorphous silicon alloy material overlying said intrinsic layer; said first and second doped amorphous silicon layers being opposite in conductivity type".

2.3 Starting from the closest prior art disclosed in document D9, the objective problem underlying the claimed invention remains - as disclosed in the opposed patent, column 1, lines 44 to 49 - to form a large area flat panel display having a high packing density (of pixels), which panel can be produced with reduced lithography control tolerances. In the Board's view, a skilled person is able to derive from the opposed patent, column 4, lines 30 to 57 that the use of a-Si p-i-n diodes provides the solution of this problem. From the limited **lateral** conductivity of the amorphous silicon layers comprised in the p-i-n diode (column 4, lines 38 to 40) and the fact that the intrinsic amorphous silicon layer of the p-i-n diode need not be etched all the way through (column 4, lines 46 to 50), a skilled person easily concludes that in an a-Si p-i-n layer sequence the characteristics of individual diodes are primarily determined by the thickness of the subsequently deposited p-, i- and n- layers and that they are less dependent on the lateral dimensions of the patterned area of each individual diode such as determined by the pattern of the photolithographic mask for etching the circuit pattern. Hence, the limited lateral conductivity - in particular in the i layer - allows to increase the tolerances of the pattern forming steps and is thereby in particular advantageous in that it allows to fabricate large area panels with uniform characteristics; see also paragraph VIII-(a) above.

2.4 All documents cited in the present case show that in the prior art a-Si p-i-n structures have exclusively been used in solar cells but not for switching pixels of a liquid panel display. From the photovoltaic conversion efficiency of an a-Si p-i-n diode for photons no conclusion can be drawn with regard to the current characteristics of such a diode in relation to an applied voltage. Energy conversion and current-switching

are based on different physical primary processes. Furthermore, it is generally known that in devices for energy conversion the lateral pattern dimensions of individual diode areas are incomparably larger than those of diodes which are to be integrated into one pixel of an image display. Hence, in the Board's view, a skilled person is not able to recognise in the use of a-Si p-i-n diodes for solar cells that the limited lateral conductivity of the intrinsic amorphous silicon region would allow to increase the tolerances of photolithographic patterning steps of a panel display without decreasing the homogeneity of the pixel properties. The Board is convinced that such effects of the intrinsic interlayer remain hidden in its practical use in a solar cell.

2.5 Documents D9 and D5 are totally silent about any tolerance problems in photolithographic patterning of display pixels and their electronic addressing means. Document D5 only mentions on page 1579 in the paragraph "fabrication" that in the fabrication of thin-film circuitry an adequate yield on a silicon substrate of useful size having the required device characteristics, has not been obtained and proposes to assemble the required matrix from a number of submatrices of reasonable area. Document D9 restricts its teaching to electrical properties of a basic unit which consists of two display elements, and only specifies electrical parameters of a single diode.

2.5.1 The Board considers - contrary to the Opponent's opinion in paragraph VII-(a) - that document D9 gives no incentive to replace a polycrystalline p-n junction diode by a diode of another type. A skilled reader derives from document D9, page 3404, paragraph 4 that the "stringent demand" of a low reverse leakage current is already realised in the device of document D9 by the

p-n structure and method of its fabrication disclosed in this document. Hence, a skilled person would continue to realise a low reverse leakage current by a deposition of p-doped polycrystalline silicon and by laser heating for drive-in of n impurites from a n dopant bearing photoresist. Furthermore, the Board does not regard it as realistic that a skilled person would isolate the criterium of a low leakage current from the additionally stated criteria such as a diode capacitance which is smaller than that of the display element, and a forward resistance which is very much smaller than the cell resistance of the display element. In practice, a skilled person would only make use of a diode structure which can be reasonably expected to satisfy all known criteria for a successful functioning of a display panel at the same time.

2.5.2 However, there is no evidence on file, that a skilled person is able to design fabrication parameters of a p^+-π-i-n^+ structure in amorphous silicon - for which a minimum reverse leakage current has been measured according to curve a' in Figure 3 of document D6 (see also paragraph VII-(c) above) - in such a way that this structure satisfies at the same time the necessary requirements with regard to capacitance and forward resistance. Document D6, page 4289, right column, paragraph 4 shows that the basic phenomena of a diode in amorphous silicon are not yet fully understood. The existing theory of the functioning of a p-n junction and a p-i-n structure in crystalline silicon is known to be inapplicable to amorphous material because of the absence of any long range order in amorphous material and the resulting complications in any theoretical approach due to the complex behaviour of the corresponding localised states in the mobility gap. The fact that the opposed patent includes within the term "amorphous" an amorphous material with crystalline

inclusions (see point VII-(b) above), does not establish the required long range order which is indispensable for the validity of generally known dimensioning rules for p-n junction and p-i-n structures in crystalline material. Hence, from the properties of polycrystaline p-n and p-i-n structures, no reliable prediction of the properties of the corresponding amorphous structures can be extrapolated.

2.5.3 In a p-n junction diode reverse blocking is known to be effected by the increase of the voltage dependent width of the depletion region between the two space charge regions of opposite polarity. In a p-i-n diode reverse blocking is known to be effected by the depletion of the voltage dependent charge carrier density in the intrinsic region. In view of these different blocking mechanisms the Opponent's interpretation of the p^+-π-i-n^+ structure of document D6 as representing a p-i-n structure (see paragraph VII-(c) above) is held to be a purely intellectual possibility of generalising the characterisation of the doping sequence. But within the framework of the disclosure of document D6, a skilled person would seriously contemplate providing a p-n junction diode with the lowest possible doping density n = 0 as a technical means forming a junction diode; i.e. a means with variable width of the depletion region. Basing the interpretation of document D6 on a different blocking mechanism such as the variable charge carrier density in the intrinsic layer of a p-i-n diode, represents in the Board's view an unallowable ex-post facto interpretation of the prior art document.

2.5.4 In view of the facts set out in paragraph 2.5.1 to 2.5.3 above, the Board is satisfied that a skilled person would not consider the p^+-π-i-n^+ structure of document D6 to form an operative diode means allowing to replace the polycrystalline p-n junction diodes in the panel display

according to document D9. Hence, the Opponent's submissions as set out in paragraph VII-(d) above are not accepted.

2.6 For the reasons set out in detail in paragraphs 2.1 to 2.5.4, the Board decides that the subject-matter of Claim 1 involves an inventive step within the meaning of Article 56 EPC.

3. Hence, it follows that granted Claim 1 is allowable. Dependent Claims 2 to 5 concern particular embodiment of the flat panel display according to Claim 1 and are, therefore, likewise allowable.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer G. D. Paterson