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D E C I S I O N
of 27 July 1995

Case Number: T 0453/94 - 3.5.2

Application Number: 89480114.1

Publication Number: 0410063

IPC: H03K 19/173

Language of the proceedings: EN

Title of invention:

Differential cascode current switch (DCCS) logic circuit family
with input diodes

Applicant:

International Business Machines Corporation

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 56

Keyword:

"Inventive step - yes, after amendment"

Decisions cited:

-

Catchword:

-



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Boards of Appeal

Chambres de recours

Case Number: T 0453/94 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 27 July 1995

Appellant: International Business Machines
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Representative: Klein, Daniel Jacques Henri
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Decision under appeal: Decision of the Examining Division of the European
Patent Office dated 28 December 1993 refusing
European patent application No. 89 480 114.1
pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: A. G. Hagenbucher
W. M. Schar

Summary of Facts and Submissions

I. The Appellant contests the decision of the Examining Division to refuse European Patent Application No. 89 480 114.1. The reason given for the refusal was that the subject-matter of the claims then on file did not involve an inventive step, having regard to document

D1: EP-A-320 555 and acknowledged prior art shown in Figure 3 of the present application.

II. During the appeal proceedings, the following prior art (which was already cited in the application) was also considered:

D3: US-A-4 760 289.

III. The Appellant filed new claims and amended description pages and drawings. In the letter dated 30 May 1995, the Appellant stated that the claims have been revised to meet the various objections raised by the Board of Appeal. The claims filed with this letter contained some obvious clerical errors. After correction of these errors (by telefax), the claims are worded as follows:

"1. An exclusive OR (XOR) logic circuit (50) of DCCS type to perform a XOR function and its complement value between IN PHASE (X51, ...) input signals and OUT OF PHASE input signals ($\bar{X}51$, ...) to generate a circuit output signal (F) and its complement (\bar{F}) at respective circuit output nodes (OUT, $\bar{O}UT$) including a first XOR circuit of a casode current switch type which is driven by first input signals (X51, Y51, $\bar{X}51$, $\bar{Y}51$) and consists of an upper (55) and a lower (54) stage connected to form a bottom stage, wherein a current source connects the common emitter node of the lower stage (54) to a second

supply voltage to supply a constant current (I0) therein;

CHARACTERIZED IN THAT

a second XOR circuit (TX531 to TX534) of a current switch type forms a top stage (56) that is cascoded and dotted with said bottom stage and consists of a pair of first and second input transistors (TX531, TX534) and a pair of third and fourth input transistors (TX532, TX533) connected in a differential amplifier configuration, so that said first and third input transistors on the one hand and said second and fourth transistors on the other hand form two independent branches and have their emitters tied together to form two common emitter nodes; the collectors of the second and third input transistors on the one hand and those of the first and fourth transistors on the other hand are connected to the respective circuit output nodes (OUT, $\bar{O}\bar{U}\bar{T}$); a pair of load resistors (RCT5, RCC5) connects said output nodes (OUT, $\bar{O}\bar{U}\bar{T}$) to a first supply voltage (VPP); and in that

a third XOR circuit is connected to the second XOR circuit and consists of:

a first logic circuit means (D531, D532, RD51, TX51 to TX54) which is connected to the base of said first and fourth input transistors and has a first AND gate (D531, D532, RD51) performing an AND function between two further Ored IN PHASE input signals (Z51 + Z52) and their Ored OUT OF PHASE input signals ($\bar{Z}51 + \bar{Z}52$); and

a second logic circuit means (D533, D534, RD52, TX55 to TX58) which is connected to the base of said second and third input transistors and has a second AND gate (D533, D534, RD52) performing an AND function between a first couple of ORed mixed IN PHASE/OUT OF PHASE signals of said further input signals ($\bar{Z}51 + Z52$) and a second couple of mixed IN PHASE/OUT OF PHASE signals of said input signals ($Z51 + \bar{Z}52$).

2. A two-bit compare logic circuit (60) of a DCCS type to perform a compare function between IN PHASE (X61, ...) input signals and OUT OF PHASE input signals ($\bar{X}61$, ...) to generate a circuit output signal (F) and its complement value \bar{F} at the circuit output nodes (OUT, $\bar{O}UT$) including a first XOR circuit of a cascode current switch type which is driven by first input signals (X61, Y61, $\bar{X}61$, $\bar{Y}61$) and consists of an upper (65) and a lower (64) stage connected to form a bottom stage; wherein a current source connects the common emitter node of the lower stage (64) to a second supply voltage to supply a constant current (I0) therein;

CHARACTERIZED IN THAT:

an AND circuit (TX631, TX632) of the current switch type forms a top stage (66) that is cascoded and dotted with said bottom stage and consists of a pair of first and second input transistors (TX631, TX632) having their emitters tied together to form a common emitter node; the collectors of these input transistors are connected to the respective circuit output nodes; a pair of load resistors (RCT6, RCC6) connects said output nodes (OUT, $\bar{O}UT$) to a first supply voltage (VPP); and in that

a second logic XOR circuit is connected to the AND circuit and consists of:

first logic circuit means (D631, D632, RD61, TX61 to TX64) which is connected to the base of said first input transistor and has a first AND gate (D631, D632, RD61) performing an AND function between two further ORed IN PHASE input signals ($Z_{61} + Z_{62}$) and their ORed OUT OF PHASE input signals ($\bar{Z}_{61} + \bar{Z}_{62}$); and

second logic circuit means (D633, D634, RD62, TX65 to TX68) which is connected to the base of said second input transistor and has a second AND gate (D633, D634, RD62) performing an AND function between a first couple of ORed mixed IN PHASE/OUT OF PHASE signals of said further input signals ($\bar{Z}_{61} + Z_{62}$) and a second couple of mixed IN PHASE/OUT OF PHASE signals of said further input signals ($Z_{61} + \bar{Z}_{62}$).

3. The logic circuit of Claim 1 or 2 wherein said first supply voltage (V_{PP}) is lower than 3.4 V."

IV. The Appellant argued essentially that a person skilled in the art would not automatically apply the level shifter devices of the SECCS (single-ended cascode current switch) logic circuit known from D1 and shown in Figure 2 of the present application to the top stage of a DCCS (differential cascode current switch) logic circuit such as shown as prior art in Figure 3 of the present application in order to add more than one logic function to be implemented in a single logic tree with reduced power supply ($V_{pp} = 3.4V$). Otherwise such an improvement would have been suggested at the time the circuit of Figure 2 was invented (December 1987) and not two years later, by an engineer of the same development

team which had developed the prior art circuit shown in Figure 3. A person skilled in the art would have considered such a combination as non-operative under low power supply. A tracking problem could exist if the transistor diode networks of two complementary level shifter devices were not matched and would have deterred the skilled person from considering such a combination. Moreover, the circuits of Figures 5 and 6 would not be obviously derivable from the available prior art.

V. The Appellant requested that the decision of the Examining Division be set aside and that a patent be granted on the basis of the following documents:

Claims: 1 to 3 filed by telefax on 24 July 1995

Description: pages 3, 6, 7, 8, 9, 11, 12, 16, 17, 19, 21 filed with the letter of 30 May 1995, received on 14 June 1995

pages 4, 9, 10, 14, filed with the letter of 14 February 1995, received on 20 February 1995

page 20 filed with the letter of 24 November 1994, received on 29 November 1994

pages 1, 2, 5, 13, 15, 18 as originally filed

Drawings: sheets 1/4 and 2/4 as originally filed
sheet 3/4 filed with the letter of 30 May 1995, received on 14 June 1995

sheet 4/4 filed with the letter of 14 February 1995, received on 20 February 1995.

Reasons for the Decision

1. The appeal is admissible.
2. The features recited in the claims now on file were all disclosed in combination in the application documents as originally filed (see especially Figures 5 and 6). The description has been adapted to the present claims. In the opinion of the Board, the amendments do not infringe Article 123(2) EPC.
3. Neither of the prior art documents D1, D3, nor the prior art acknowledged with reference to Figures 1 to 3 of the present application, shows all the features recited in Claim 1 or Claim 2. Thus, the subject-matter of Claims 1 and 2 is novel within the meaning of Article 54 EPC.
4. In the opinion of the Board, the closest prior art is the exclusive OR (XOR) logic circuit shown in Figure 4 of D3. This XOR circuit has all the features indicated in the preamble of Claim 1. Since the function of a XOR circuit can be interpreted as comparing two bits for inequality (antivalence) and since the compare logic circuit according to Claim 2 further develops the XOR circuit structure of Figure 4 of D3, Claim 2 starts in its preamble also from this prior art.

The prior art XOR circuit generates the XOR-function and its complement for only two input signals (A, B corresponding to Y51, X51) and their complements (-A, -B corresponding to $\bar{Y}51$, $\bar{X}51$).

There is, however, a need for more efficient logic circuits connecting quickly more than two input signals and operating at low supply voltage levels (3.4V to 3.6V) imposed by modern bipolar technologies.

Hence, the problems underlying the subject-matter of Claims 1 and 2 are seen in the further development of the known XOR circuit in such a way that more than two input signals are quickly connectable at low supply voltages for generating an XOR function (Claim 1) or for (equivalence) comparing the result of two two-bit XOR functions (Claim 2).

5. These problems are solved by the features specified in the characterising parts of Claims 1 and 2 respectively.

Both solutions make use of only three stages (Figure 5: 54, 55, 56; Figure 6: 64, 65, 66) in order to allow operation at low power supply voltages (e.g. 3.4V to 3.6V) imposed by modern bipolar technologies. The solution according to Claim 1 adds to the known XOR circuit (in Figure 5: stages 54 and 55) a third stage (56) which combines by means of an XOR-function the result of the known XOR circuit for two input signals (X51, Y51) and of a further XOR function for two further input signals (Z51, Z52). The solution according to Claim 2 adds to the known XOR circuit (in Figure 6: stages 64, 65) a third stage (66) which combines by means of an AND-function the result of the known XOR circuit for two input signals (X61, Y61) and of a further XOR function for two further input signals (Z61, Z62).

6. As explained in the present description, a cascode structure of circuits has been developed for implementing efficient logic functions at high speed. There are two main logic circuit families of cascode structure, namely a single ended cascode current switch (SECCS) circuit family and a differential cascode current switch (DCCS) circuit family. The present invention belongs to the latter one as does the XOR circuit of Figure 4 of D3. It is furthermore set out in

the present description that DCCS circuits may be easily derived from SECCS circuits and that a SECCS circuit (shown in Figure 2 of the present application and known from D1) has already been designed with three stages for operating at a low power supply voltage, implementing additional logic functions at the highest stage in order to extend the logic efficiency of the circuit.

The Appellant's argument that DCCS circuit families are more problematic than SECCS circuits, because they require a balanced circuit layout of the two distinct branches in order to avoid a problem of tracking, is generally accepted. Nevertheless the present application acknowledges an easy derivability of DCCS circuits from a SECCS circuit structure. The Board concludes therefrom that a person skilled in the art would also try to apply the teaching of D1 to the circuit shown in Figure 4 of D3 if he wanted to improve the efficiency of the known XOR circuit for combining more than two input signals at low power supply. But the invention as now claimed goes further than these general considerations.

The subject-matter of Claim 1 is distinguished from the prior art according to Figure 4 of D3 by

- (a) extending the two-bit XOR-function to a four-bit XOR function;
- (b) adding a second XOR circuit (as a third stage on top of the upper stage of the known XOR circuit;
- (c) implementing a further XOR function by a symmetrical arrangement of first and second logic circuit means connected as specified in the claim to the input transistors of the second XOR circuit, wherein the diode resistor combinations (D531, D532, RD51; D533, D534, RD52) operate as

complementary level shifter devices. Furthermore, the skilled person recognises that the symmetrical circuit arrangement ensures that the propagating times are equal.

The subject-matter of Claim 2 is distinguished from Figure 4 of D3 by

- (a) extending the known two-bit (antivalence) compare circuit to an equivalence circuit comparing the result of two exclusive OR functions;
- (b) adding an AND circuit as a third stage on top of the upper stage of the known XOR circuit;
- (c) implementing a further XOR function by a symmetrical arrangement of first and second logic circuit means connected as specified in the claim to the input transistors of the AND circuit, wherein the diode resistor combinations (D631, D632, RD61; D633, D634, RD62) operate as complementary level shifter devices. Furthermore, the skilled person recognises that the symmetrical circuit arrangement ensures that the propagating times are equal.

The Board is of the opinion that even a combined consideration of D1 and D3 (corresponding to Figure 2 of the present application) together with the other prior art acknowledged with reference to Figures 1 and 3 of the present application does not render the claimed solutions obvious. Even if the need for feature (a) arises out of practise and feature (b), namely the addition of a third stage with further inputs would follow from D1, the available prior art would not teach feature (c), namely how to implement the third stage with specific input logic to arrive at complementary level shifter devices with equalised propagating times.

Hence, in the Board's judgement the subject-matter of Claims 1 and 2 involves an inventive step in the sense of Article 56 EPC. Dependent Claim 3, defining the upper limit for the supply voltage, is likewise allowable.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a patent according to the Appellant's request (see paragraph V above), with correction of the clerical errors in Claims 1 and 2, i.e. in the form indicated in paragraph III above.

The Chairman:

The Registrar:

M. Kiehl

W. J. L. Wheeler