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D E C I S I O N
of 15 May 1995

Case Number: T 0457/94 - 3.5.1

Application Number: 84903564.7

Publication Number: 0157882

IPC: G05B 19/405

Language of the proceedings: EN

Title of invention:
Numerical control apparatus

Patentee:
FANUC LTD

Opponent:
Robert Bosch GmbH

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0457/94 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 15 May 1995

Appellant: (Opponent)
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Representative:
-

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Decision under appeal: **Decision of the Opposition Division of the European Patent Office dated 25 March 1994 rejecting the opposition filed against European patent No. 0 157 882 pursuant to Article 102(2) EPC.**

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: C. G. F. Biggio
G. Davies

Summary of Facts and Submissions

I. By a decision dated 25 March 1994, the Opposition Division rejected the opposition lodged against European patent No. 0 157 882, granted upon patent application No. 84 903 564.7.

II. The decision was based on the patent as granted; the sole claim thereof reads:

"A control system comprising a processing unit (1), a memory (2), an input-output means (3), and a display means (4) operable to display simultaneously in a single picture the conditions or positions of a plurality of control elements with respect to a common time scale in a first area (42) of a display screen for displaying the sequential progress of information relating to said control elements, the display screen having a second area (43) for displaying display conditions relating to the information displayed in the first area (42), characterised in that

(a) the control system is a numerical control system employable for numerically controlling a machine tool and comprises a programmable controller (5) to supplement the function of the processing unit (1);

(b) the input-output means (3) comprises a first input means (31) for inputting to the processing unit (1) the address numbers of a plurality of selectable information elements to be displayed in said first area (42), which address numbers may be remote from one another in a program but may relate to one another from a functional viewpoint;

(c) the processing unit (1) comprises a first selector (11) for these address numbers and the display means (4) are operable to display these address numbers in a third area (41) to identify the

control elements being indicated in the first area (42);

(d) the input-output means (3) comprises a second input means (33) for inputting to the processing unit (1) a selectable time scale for the display in the first display area (42), and the processing unit (1) comprises a second selector (12) for this time scale;

(e) the input-output means (3) comprises a third input means (32) for inputting to the processing unit (1) the address number of a display trigger information element and the processing unit (1) comprises a third selector (13) for this display trigger information element;

(f) the input-output means (3) comprises a fourth input means (33) for inputting to the processing unit (1) a command for selecting either a set of repetitive pictures or a one shot non-repetitive picture, and the processing unit (1) comprises a conducting device for conducting said command; and

(g) the input-output means (3) comprises a fifth input means (35) for inputting the delay time for which the commencement of display is delayed after the corresponding trigger signal is issued, and the processing unit (1) comprises a fourth selector (15) for said delay time" (subdivision of the claim into single features (a) to (g) carried out by the Board).

III. The Opposition Division considered that the subject-matter of the above-quoted claim 1 involved an inventive step over the teaching from the following prior art documents:

D2: DE-A-2 950 102,

D5: Zeitschrift Elektronik, No. 10, 1982, title page and pages 54 to 56,

D6: Zeitschrift Elektronik, No. 9, 1982, page 13,

D7: Zeitschrift Elektronik, No. 8, 1983, page 79,

D8: Zeitschrift Elektronik, No. 11, 1982, page 54,

D9: Zeitschrift Elektronik, No. 6, 1983, pages 101 to 104,

D10: Zeitschrift Elektronik, No. 8, 1983, Ulrich Niermann: "Logikanalyse wird anwenderfreundlicher", pages 81 to 84, and

D11: Zeitschrift technica, No. 17, 1982, page 1404, "Erleichtertes Programmieren mit Bildschirm".

IV. The appellant (opponent) lodged an appeal against the decision of the Opposition Division on 27 May 1994, paying the appropriate appeal fee the same day.

Grounds of Appeal were filed on 23 July 1994.

The appellant requested that the appealed decision be set aside, that the patent be revoked and, subsidiarily, that oral proceedings be held.

V. On 15 December 1994, the respondent (patentee) filed observations on the Grounds of Appeal, requesting that the appeal be dismissed and, subsidiarily, that oral proceedings be held.

VI. Oral proceedings were held on 15 May 1995.

VII. In writing and at the oral proceedings, the appellant followed two different lines of argument.

Firstly the claim was stated to be not new, having regard to document D5.

In order to elucidate this, the appellant handed to the respondent and to the Board a copy of the claim in which the latter was divided up into separate features in a fashion similar to that followed by the Board under foregoing Item II. These features were one after the other argued to be known from document D5.

In particular, the preamble of the claim combined with feature (a) of the characterising clause indicated that the invention as claimed concerned the same type of control system the logic analyser according to D5 was provided for.

The system described in this document possessed, according to the appellant, also the features: "Address", "Time scale", "Trigger" and "Display modus", as reflected in features (b) to (f) in the Board's notation.

Although the feature: "Delay", reflecting feature (g), was maybe not explicitly known from D5, it was very trivial, to such an extent that it could not cause the subject-matter of the claim to be new, with regard to document D5.

Secondly, the appellant argued as follows:

The alleged invention merely added to a known CNC control system, as admitted to be known in the patent at issue, a logic analyser which was shown to be known by the various prior art documents on file.

Document D11 disclosed the intimate connection of a logic analyser with a numerically programmable system, for the purpose of "on-line" programming the latter, so that the person skilled in the art would have considered as obvious to associate and even integrate such a logic analyser into a known CNC system, for the purpose of programming and even "on-line" monitoring the functioning of said CNC system. A similar teaching was also disclosed by document D2, since it dealt with the monitoring of a process in which a plurality of conditions or positions of a plurality of control elements were displayed with respect to a common time scale.

The article by Klaus Link "Der Logikanalysator", on page 82 of document D10, indicated, moreover, that there was a development of the logic analysers tending to "specialise" such devices, which were originally conceived as "universal" measuring instruments, so that it was to be expected that the logic analyser of the future would have to be integrated into numerical systems.

Feature (a) of the characterising clause of the sole claim should, accordingly, be considered as not providing any contribution to an inventive step with respect to the subject-matter of said claim.

Features (b) to (g) of the characterising clause of the sole claim merely prescribed that the device resulting from the obvious incorporation of a numerical analyser into a CNC system should comprise:

- the facility of addressing a plurality of selectable information elements to be displayed in a first area of the display screen, by inputting to the processing unit suitable address numbers

through suitable input means and the capability of displaying said suitable address numbers in a further area of the display screen to identify the control elements being displayed in said first area of the display screen (features (b) and (c));

- the facility of inputting to the processing unit a selectable time scale for the display in the first display area; said time scale being input through suitable selecting means (feature (d));

- the facility of inputting, through suitable selecting means, a selectable display trigger information to the processing unit (feature (e));

- the facility of inputting to the processing unit a suitable command for selecting a suitable display modus and the capability of conducting the displays according to said selected display modus (feature (f)); and

- the facility of inputting, through suitable selecting means, a suitable delay time for which the commencement of display is delayed after the corresponding trigger signal is issued (feature (g)). The various prior art documents on file, and in particular figure 5 on page 55 of document D5, showed that the known logic analysers comprised facilities and capabilities of the same kind, so that it would have been obvious, for the person skilled in the art, to define the specific facilities and capabilities defined in features (b) to (g) of the sole claim; said facilities and capabilities being only more specifically adapted to the functioning of a logic analyser in connection with a known CNC system.

VIII. In writing and at the oral proceedings, the respondent made substantially the following submissions.

The point of the invention was that the programmable controller was integrated with the processing unit; integration meaning that the programmable controller had access to the internal busses, whereas the disclosures of the prior art merely referred to external logic analysers connected to, or at the most, plugged into numerical control devices.

The integration in a CNC system of the facilities and capabilities of a logic analyser, as according to the sole claim, was neither disclosed, nor even hinted at, by the various prior art documents on file, which, indeed, merely dealt with external logic analysers connected to, or at the most, plugged into numerical control devices. Document D2 was a typical example of such a technique, where the logic analyser was merely plugged into a signal mixer and had, consequently, no access to the internal busses of the numerically controlled system, but merely access to external information.

Document D11 dealt with the association of logic analysers with programmable numerical control systems, but merely for the purpose of programming said numerical control systems, whereby both "off-line" and "on-line" functioning of such associations were envisaged. No monitoring of said numerical control systems, during their operation, was envisaged in said document.

The teaching effectively disclosed by documents D5 and D10 was restricted to the performances of logic analysers, as used according to their original

conception, i.e. as universal measuring devices susceptible of being externally connected to the numerical control systems they should analyse.

As to the article by Klaus Link "Der Logikanalysator", on page 82 of document D10, it merely summarized the past uses of logic analysers and speculated on the future possible development and uses thereof. Even if it might be inferred that said article "envisaged" future uses, requesting an integration of the logic analyser in the numerical control systems to be analysed, the teaching it provided on said future uses was far from even suggesting features (b) to (g), as specified in the sole claim, of the control system according to the invention.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Novelty*

The various prior art documents on file disclose display means operable to display simultaneously in a single picture the conditions or positions of a plurality of control elements with respect to a common time scale.

However none of said documents discloses such a display means in a numerical control system (CNC) employable for numerically controlling a machine tool as set forth in the sole claim.

This applies in particular to document D5, on the basis of which the appellant made a novelty objection against the subject-matter of the sole claim.

In the opinion of the Board, in fact, this document does not disclose the features (b) to (g) of the claim. It does not disclose "real" addressing as required by the claim. As the respondent put forward, D5 does not disclose the claimed integrated system. The addresses shown in the photograph on the front cover, A7...A0, clearly suggest a limited address range defined by some sort of external interface. It itself has only 16 data channels. Aside from the signals directly available to the interface, the only memory it can have access to is its own.

On the contrary, feature (b) of the claim of the contested patent specifies that the address numbers input to the processing unit (1) are of such a character that they "may be remote from one another in a program, but may relate to one another from a functional viewpoint"; the processing unit (1) according to feature (c) comprising a selector (11) for these address numbers.

Although the cited phrase seems to mention only an example of the kind of address numbers which may be utilised in the system as claimed, the Board is satisfied that this phrase nevertheless specifies that the system according to the claim is such that it must be suitable for address numbers of this kind. In the Board's view, this feature shows in particular that the claim concerns indeed an integrated system in which the monitoring facility can be directly connected to the CPU bus and can measure any sort of internal signal, as the Opposition Division pointed out correctly in its decision under reason 3.8. The Board would prefer to add

to the last part of this sentence the words "in principle", i.e. if the corresponding addresses have been input beforehand to the processing unit (1).

All this constitutes a major difference compared to the logic analyser according to D5, which is plugged in and, thus, only has access to the signals available to the external interface.

Thus the subject-matter of the sole claim is new with regard to D5.

Document D2, acknowledged in the contested patent, deals with the monitoring of a process in which a plurality of conditions or positions of a plurality of control elements with respect to a common time scale are displayed, whereby the logic analyser is merely plugged into a signal mixer and has, consequently, no access to the internal busses of the numerically controlled system, but merely access to external informations (see Figure 2).

Document D11 deals with the association of logic analysers with programmable numerical control systems, but merely for the purpose of programming said numerical control systems, whereby both "off-line" and "on-line" functioning of such associations are envisaged. No monitoring of said numerical control systems, during their operation, is envisaged in said document.

The teaching effectively disclosed by documents D5 and D10 is restricted to the performances of logic analysers, as used according to their original conception, i.e. as universal measuring devices susceptible of being externally connected to the numerical control systems they should analyse. Even Figure 5, on page 55 of document D10, does not disclose

anything more than the standard features: MODE SELECTION, CLOCK SELECTION, TRIGGER SELECTION, TIME DISPLAY and STATE DISPLAY of a standard logic analyser.

The article by Klaus Link "Der Logikanalysator", on page 82 of document D10, indicates, indeed, that there was a development of the logic analysers tending to "specialise" such devices, which were originally conceived as "universal" measuring instruments, so that it could be inferred that it "envisages" the logic analyser of the future as being integrated ("eingebunden") into numerical systems to be analysed. The teaching it provides on said future uses is, however, far from defining and even suggesting, for a future control system according to said future uses, such features as features (b) to (g), as specified in the sole claim.

Thus none of the cited documents discloses a system as set forth in the sole claim.

3. *Inventive step*

As established under the foregoing reason 2, the system as claimed is mainly distinguished from the prior art in that it concerns an integrated system in which the monitoring facility can be directly connected to the CPU bus and can, in principle, measure any sort of internal signal.

None of the prior art documents cited goes beyond a logic analyser which is plugged in and thus has only access to signals available to the external interface, as disclosed by D5.

The invention, as claimed, enables a much greater flexibility in the choice and the number of points to be monitored in the control system. It is clear to the Board that here the control system according to the sole claim does not result from the mere association or juxtaposition of a known CNC control system, as admitted in the patent at issue, with a logic analyser which is shown to be known by the various prior art documents on file.

There is not the slightest hint, in the prior art, to change from a logic analyser of the kind disclosed by D5 to an integrated system as claimed; not even in the speculations about possible future developments by Klaus Link in D10. This article does not contain any indication that the structure of the logic analyser itself will change. With regard to the application of microprocessors in connection with logic analysers, the article does not arrive at a specific conclusion and the final sentence of this article only indicates that the logic analyser may be embedded in a system and even be connected to a local network. These phrases, however, say nothing about the way in which the values to be monitored are obtained, but seem only to say something about what can be done, once these values are available on some transmission channel.

The present invention, on the contrary, concentrates on the way data to be monitored are collected.

Even assuming that the aim of achieving the said greater flexibility would have been a natural one for a person skilled in the art, it was still not necessarily obvious that said skilled person would have then chosen, as a solution, the integration of the system, because, in the view of the Board, the realisation of an integrated

system as claimed required a quite different and new approach on the side of the skilled person concerned with logic analysers.

The appellant has argued that, once it had been decided that the system should be integrated, the various features of the claim would have been logical consequences of said decision to integrate; the latter being **a priori** obvious in his view.

In the foregoing the Board has made it clear that said decision to integrate was not obvious and has given reasons why.

But even if, for the sake of argument, said decision to integrate had been obvious, then still the features of the claim would not have immediately followed in all their specific details, as the opposition division correctly pointed out in great detail in reason 3.6 of its decision, in particular with regard to D5 which, in fact, is the most detailed of the cited documents.

Under these circumstances there is no need for the Board to repeat the opposition division's reasoning.

The Board is consequently of the opinion that

- the subject-matter of the sole claim involves an inventive step pursuant to Article 56 EPC, and

- the invoked ground for opposition pursuant to Article 100 EPC does not prejudice the maintenance of the patent at issue, as granted.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Kiehl P. K. J. van den Berg