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D E C I S I O N
of 22 April 1997

Case Number: T 0594/94 - 3.4.1

Application Number: 88117298.5

Publication Number: 0312975

IPC: H01L 23/538

Language of the proceedings: EN

Title of invention:
Semiconductor chip package

Applicant:
SAMSUNG ELECTRONICS CO., LTD

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes, after amendment)"

Decisions cited:
-

Catchword:
-

Case Number: T 0594/94 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 22 April 1997

Appellant: SAMSUNG ELECTRONICS CO., LTD.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 10 March 1994 refusing European patent application No. 88 117 298.5 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. D. Paterson
Members: H. J. Reich
Y. J. F. van Henden

Summary of Facts and Submissions

I. European patent application No. 88 117 298.5 (publication No. 0 312 975) was refused by a decision of the Examining Division.

II. The reason given for the refusal was that the subject-matter of claim 1 filed on 29 September 1993 did not satisfy the requirements of Articles 52(1) and 56 EPC having regard to document:

D3: US-A-4 551 746.

The Examining Division took the following view: The subject-matter of claim 1 is distinguished from the package disclosed in document D3 by two obvious features: The first distinguishing feature - that the large area conductor areas are provided on the same surface which supports the connector pads - would be obvious in view of the teaching in document D3, column 20, lines 1 to 9 and column 19, lines 61 to 68 disclosing that the power and ground planes can be located throughout the various layers of the carrier. The second distinguishing feature - that any selectively programmed connector pad remains also connected to a corresponding signal connector - would not be inventive since a corresponding extension of vias would fall into the discretional routine measures of a skilled person. Also dependent claims 2 to 11 cannot be seen to impart inventiveness to any of the claims to which they refer, as outlined in the communication dated 27 July 1992, point 3. In particular, nothing inventive can be seen in the formation of ring-like power or ground lines. The formation of metallisation rings per se is known in the art and its advantages are well understood.

III. The appellant lodged an appeal against this decision. With the statement of grounds of appeal the appellant filed a new set of claims, including features from dependent claims, - in particular that "large area ring-shaped conductor areas are provided around the contour of the semiconductor chip and surround said connector pads."

IV. During the appeal proceedings, on 20 December 1995, the present European patent application has been transferred from "Honeywell Inc." to "Samsung Electronics Co., Ltd.".

V. In a communication dated 17 October 1996 pursuant to Article 110(2) EPC, the Board raised objections under Article 84 EPC and Rules 29(1)(a) and 27(1)(c) EPC and proposed corresponding amendments. In reply to the Board's communication the new appellant filed two completely reworded sets of claims as main and subsidiary requests, maintaining largely the characterising features suggested by the Board. Following a telephone consultation between the rapporteur and the new appellant's representative on 9 April 1997, the appellant now requests that a patent be granted according to his main request on the basis of the following documents:

Claims: 1 to 10 filed on 24 March 1997;
Description: pages 1 to 10 filed on 24 March 1997; with the amendments on pages 4 and 6 requested 9 April 1997;
Drawings: Figures 1, 1a and 2 to 13 according to EP-A-0 312 975;

or that a patent be granted on the basis of his auxiliary request filed on 24 March 1997.

VI. Claim 1 of the main request reads as follows:

"1. A semiconductor chip package comprising:

(a) a plurality of connector pads (26) located on a first surface of the package and arranged about the periphery of a semiconductor chip (24), each pad being adapted for interconnection with the semiconductor chip;

(b) a plurality of electrical connectors (22) located on a second surface of the package, some of the electrical connectors (22) being dedicated power or ground connectors (22) and others being signal connectors.

(c) a plurality of signal connection means (28, 30) providing an electrically conductive path between an individual connector pad (26) and a corresponding individual signal connector (22); and

(d) a plurality of electrical connection means (28, 32 to 48) comprising conductive paths for selectively connecting any connector pad (26) to one of the power or ground connectors; the electrical connection means comprising at least two large area conductor areas (32 to 40).

characterised in that:

(e) at least two large area conductor areas (34 to 40) are ring-shaped, provided on or beneath the first surface and, in plan view, are arranged around the contour of the semiconductor chip (24) and surround the connector pads (26)."

Claims 2 to 10 of the main request are dependent on claim 1.

VII. In support of his requests the appellant argued essentially as follows:

(a) Claim 1 covers both, the embodiment in Figures 4 to 13 with the ring-shaped large area conductor areas **on** the first surface and the embodiment in Figures 1 to 12 with the ring-shaped large area conductor areas **beneath** the first surface. Both embodiments have the advantage that said ring-shaped areas allow to program pads for use with power or ground plane independent of the site of vias within the package. According to Figure 13, chip pads to be connected to power or ground can be directly connected to a desired power or ground ring; see the original description page 9, lines 9 to 16. Having regard to the corresponding structure in Figures 1 to 3, connector pads 26 are programmed by simply changing the shape of the power of ground pads 32 in layer 2 so that different vias 28 between the connector pads 26 and pads 32 or between pads 32 and rings 34 to 40, are selected. No alteration in the position of vias 28 is necessary; see the original description page 6, lines 1 to 7.

(b) A ring-shaped configuration of large area power source and ground connections is not derivable from the relevant prior art. Its use for eliminating the necessity of package tooling for new chip designs implies the required inventive step.

Reasons for the Decision

1. The subject-matter of claim 1 of the main request is disclosed in original claims 1 and 2 and in original

Figures 1, 3 and 13 with the corresponding description. Claim 2 is disclosed in Figures 2 and 3 in combination with the original description page 6, lines 8 to 15 and page 7, lines 24 to 39. Claim 3 is based on Figure 13. Claims 4 to 6 are based in particular on Figures 2 and 4 to 11. Claims 7, 8 and 10 consist of features derivable from Figures 4, 8, 10 and 11. Claim 9 is disclosed in Figure 6. There is, therefore, no objection to the new set of claims of the main request under Article 123(2) EPC.

2. *Novelty*

2.1 Document D3 discloses in the wording of claim 1:

"A semiconductor chip (see D3, 51 in Figures 17 and 25) package comprising;

(a) a plurality of connector pads (118 and 121 in Figures 17 and 22) located on a first surface (114 and 116 in Figure 25) of the package and arranged about the periphery of a semiconductor chip, each pad being adapted for interconnection with the semiconductor chip (Figures 17 and 25);

(b) a plurality of electrical connectors (132, 130 in Figures 24 and 25; column 18, lines 27 to 29) located on a second surface (128 in Figure 25) of the package, some of the electrical connectors being dedicated power (130 at castellations 108a in Figure 24; column 16, lines 13 to 15) or ground connectors (130 at castellations 108b in Figure 24; column 16, lines 43 to 45) and others being signal connectors (130 at castellations 108 in Figure 24; column 18, lines 29 to 33);

(c) a plurality of signal connection means (108 in Figure 22) providing an electrically conductive

path between an individual connector pad (118 in Figure 17) and a corresponding individual signal connector (130, 132 in Figure 24); and

(d) a plurality of electrical connection means (108a, 108b in Figure 22) comprising conductive paths for selectively connecting any connector pad to one of the power or ground connectors; the electrical connection means comprising at least two large area conductor areas (121 in Figures 17 and 22)".

2.2 The subject-matter of claim 1 differs from the package disclosed in document D3 in the features defined by the characterising part of claim 1, i.e in particular in ring-shaped large area power or ground connectors. Power or ground connectors of such geometrical shape are not disclosed in any of the documents cited in the European Search Report.

2.3 Thus, the subject-matter of claim 1 is considered new in the sense of Article 54 EPC.

3. *Inventive step*

3.1 Starting from the closest prior art semiconductor chip package according to document D3, the objective problem underlying the present invention is to produce a non-specialised semiconductor chip package wherein the local arrangement of connector pads to existing signal, power and ground paths within the package can easily be adapted in order to be made compatible with various different patterns of signal, power and ground pads in new chip designs; see the original description, page 1, line 13 to page 2, line 16.

3.2 This problem is solved according to the characterising part of claim 1 in that

"at least two large area conductor areas (34 to 40) are ring-shaped, provided on or beneath the first surface and, in pane view, are arranged around the contour of the semiconductor chip (24) and surround the connector pads."

3.3 The Board regards the statement of the Examining Division in its communication dated 27 July 1992, point 3 - that the formation of metallization rings is per se known - to be no relevant evidence for the fact that ring-shaped power and ground lines are generally known in the art of semiconductor chip packages. Such a finding contradicts moreover the result of the European Search Report. There is no document cited against original claim 2 specifying the subject-matter of original claim 1 in that is comprises: "at least one first (34, 38) and second (36, 40) power or ground rings". The appellant contests the fact that the geometrical structure and arrangement of power and ground connections as claimed in the characterising part of claim 1 is disclosed in the cited prior art or represents general knowledge. Hence, the Board finds that - in view of the evidence on file - the prior art does not suggest to a skilled person to avoid package tooling for new chip designs by ring-shaped power and ground lines which are arranged around the contour of the chip.

3.4 In the closest prior art according to document D3 the power and ground lines extend in radial direction and surround the chip in form of rays starting at the contour of the chip; see for instance Figure 22. A similar ray-like arrangement is disclosed in Figure 3 of Solid State Technology, volume 27, No. 1, January 1984, pages 119 to 122 (D2). Intermediate parts of large area power and ground lines on internal layers within the package - such as disclosed in document D3 and in the remaining documents cited in the European

Search Report - have the shape of square or rectangular areas.

3.5 In the Board's view, a skilled person cannot be regarded as able to foresee that a geometrical structure of power and ground lines as claimed in the characterising part of claim 1 makes the programming of pads for use with power or ground independent from the site of vias within the package.

3.6 For the reasons set out above in paragraphs 3.1 to 3.5, the subject-matter of claim 1 of the main request is considered to involve an inventive step in the sense of Article 56 EPC.

4. Thus, claim 1 of the main request satisfies Article 52(1) EPC. Claims 2 to 10 of the main request concern particular embodiments of the semiconductor chip package claimed in claim 1 and are, therefore, also allowable.

5. Under these circumstances, the appellant's auxiliary request needs no consideration.

Order

For these reasons it is decided that:

1. The decision of the Examining Division is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the appellant's main request (see paragraph V above).

The Registrar: The Chairman:

M. Beer G. D. Paterson