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D E C I S I O N
of 11 March 1999

Case Number: T 0596/94 - 3.4.1

Application Number: 88310285.7

Publication Number: 0315422

IPC: H01L 27/10

Language of the proceedings: EN

Title of invention:
Semiconductor memory device having an ohmic contact between an aluminum-silicon alloy metallization film and a silicon substrate

Applicant:
Fujitsu Limited

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 123(2), 54, 56

Keyword:
"Amendments - added subject-matter (no)"
"Novelty (yes)"
"Inventive step (yes)"

Decisions cited:
T 0241/88, T 0169/83

Catchword:

-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0596/94 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 11 March 1999

Appellant: Fujitsu Limited
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 2 March 1994 refusing European patent application No. 88 310 285.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. Davies
Members: G. Assi
M. G. L. Rognoni

Summary of Facts and Submissions

I. The appellant (applicant) lodged an appeal, received on 28 April 1994, against the decision of the Examining Division, dispatched on 2 March 1994, refusing the European patent application No. 88 310 285.7 (EP-A-0 315 422). The fee for the appeal was paid on 28 April 1994. The statement setting out the grounds of appeal was received on 12 July 1994.

In its decision, the Examining Division held that the application did not meet the requirements of Article 123(2) EPC as well as of Articles 52(1) and 56 EPC, having regard to the following documents:

(D1) IEEE Journal of Solid-State Circuits, vol. SC-19, no. 5, October 1984, IEEE, New York (US), pages 596 to 602; D. Kantz et al., "A 256K DRAM with descrambled redundancy test capability", and

(D2) Thin solid films, vol. 120, no. 4, October 1984, Elsevier Sequoia, Lausanne (CH), pages 257 to 266; F. Neppl et al., "A $TaSi_x$ barrier for low resistivity and high reliability of contacts to shallow diffusion regions in silicon".

II. The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: No. 1 to 7 as filed with the letter of 26 November 1998,

Description: Pages 1, 5 to 7, 9 to 12 as originally filed,
Page 2, 3 as filed with the letter of 26 November 1998,
Page 4, 8 as filed with the letter of 12 July 1994,

Drawings: Sheets 1/3 to 3/3 as originally filed.

Furthermore, the appellant requested that oral proceedings be held in the event that the above-mentioned request should not be granted.

III. The wording of claim 1 reads as follows:

"1. A semiconductor memory device comprising a silicon substrate (11) and having a memory cell portion and a peripheral circuit portion, the memory cell portion comprising a memory cell array (110, 111) which includes a plurality of memory cells having word lines and memory cell capacitors, and having a first insulation film (20) of silicon dioxide, with a first contact hole (31) formed in the first insulation film and a first metallization film (40) formed on the first insulation film, the first metallization film including a polysilicon film (21) and a refractory metal silicide film (22) which are stacked in this sequence, the first metallization film constituting at least bit lines of said memory cell portion which are connected to said substrate via said first contact hole (31);

characterized in that the device further comprises a second insulation film (17) of silicon dioxide upon which is formed the first insulation film (20), the

peripheral circuit portion having a second contact hole (33, 34), the first and second contact holes (31, 33, 34) being formed through the second insulation film (17); in that said first metallization film contacts the silicon substrate (11) through the second contact hole (33,34) so as to further constitute a barrier layer (50, 60) in said peripheral circuit portion which is formed in said second contact hole (33, 34) and around a periphery thereof such that said polysilicon film (21) is in contact with said second insulation film (17); and in that a second metallization film (29, 30) of an alloy of aluminum and silicon overlies the barrier layer (50, 60) in the second contact hole (33, 34) whereby it is in contact with said refractory metal silicide film (22), said second metallization film constituting wiring of said peripheral circuit portion."

Claims 2 to 7 are dependent claims.

IV. The appellant argued essentially as follows:

Regarding Article 123(2) EPC:

The Examining Division's first objection concerned the feature that the first metallization film - constituting a barrier layer in the peripheral portion - was formed in the second contact hole and **around a periphery thereof**. The basis for this feature was provided by Figures 3A and 3B of the application. No indication was given in the application as filed that the feature improved the adhesion of the barrier layer to the underlying layer. However, the purpose of this feature was not primarily to achieve this advantage,

but rather to provide an effective barrier layer. The advantage of obtaining improved adhesion should be considered as a "bonus effect".

Furthermore, the Examining Division objected that, although amendments to claim 1 concerning the definition of the first and second insulation films had a basis in the embodiments according to Figures 3A and 3B, these amendments had been taken out of their proper context of essential features. This objection resulted from a misinterpretation of the meaning of the expression "essential features". A distinction should be drawn between "essential features" of a semiconductor memory device, i.e. features required for any such device to function, and "essential features" of an invention. Only the latter kind of "essential features" were relevant to the claims.

Regarding Article 56 EPC:

Both the cited documents D1 and D2 had teachings which were different from the present invention.
D2 addressed the same problem as the present invention, i.e. Si precipitation at an ohmic contact between an Al-Si metallization and silicon. The solution disclosed was to provide a barrier layer of tantalum silicide. In the event that the skilled person contemplated the use of additional layers in the barrier layer, this would not lead to the double-layer structure as claimed, because D2 taught that any additional layer should be on top of the metal silicide, not below it.

D1 disclosed the use of polycide for bit lines and gate electrodes of memory cell transistors. Bit lines, in

particular, had special requirements, i.e. low resistance and low capacitance, which were different from those of a barrier layer having to provide for effective prevention of diffusion between adjacent layers. Thus, the skilled person would have no reason to think that a bit line polycide would make an effective barrier.

Reasons for the Decision

1. The appeal is admissible.

2. *Article 123(2) EPC*

2.1 As compared with claim 1 as originally filed, the amended claim 1 includes the following further features, which are numbered as well as underlined in the wording of the claim:

A semiconductor memory device comprising a silicon substrate (11) and having a memory cell portion and a peripheral circuit portion, the memory cell portion comprising a memory cell array (110, 111) which includes a plurality of memory cells having word lines and memory cell capacitors(1), and having a first insulation film (20) of silicon dioxide(2), with a first contact hole (31) formed in the first insulation film(3) and a first metallization film (40) formed on the first insulation film, the first metallization film including a polysilicon film (21) and a refractory(4) metal silicide film (22) which are stacked in this sequence, the first metallization film constituting at least bit

lines of said memory cell portion which are connected to said substrate via said first contact hole (31)[5]; characterized in that the device further comprises a second insulation film (17) of silicon dioxide upon which is formed the first insulation film (20)[6], the peripheral circuit portion having a second contact hole (33, 34), the first and second contact holes (31, 33, 34) being formed through the second insulation film (17)[7]; in that said first metallization film contacts the silicon substrate (11) through the second contact hole (33,34) so as to further constitute a barrier layer (50, 60) in said peripheral circuit portion[8] which is formed in said second contact hole (33, 34) and around a periphery thereof[9] such that said polysilicon film (21) is in contact with said second insulation film (17)[10]; and in that a second metallization film (29, 30) of an alloy of aluminium and silicon overlies the barrier layer (50, 60) in the second contact hole (33, 34) whereby it is in contact with said refractory metal silicide film (22), said second metallization film constituting wiring of said peripheral circuit portion[11].

The amendments (1) to (11) are supported by the original disclosure. In particular:

(1) See claim 2, page 9, lines 7, 8, 22 to 24, page 11, lines 13 to 15, Figure 3B.

(2) See page 9, lines 25, 26.

(3) See page 9, lines 31 to 35.

(4) See claim 4, page 10, lines 21 to 24.

(5) See page 10, lines 5 to 11, Figure 3B. The expression "at least" is justified by the fact that the first metallization film constitutes bit lines 40 as well as barrier layers 50, 60.

(6) See page 8, lines 29 to 32, page 9, lines 25 to 27, Figure 3B.

(7) See page 9, lines 27 to 35, Figures 3A, 3B.

(8) See page 10, lines 5 to 15, Figures 3A, 3B.

(9) See Figures 3A, 4.

(10) See Figure 3A, 4.

(11) See page 11, lines 10 to 15, Figure 3A.

2.2 In the decision under appeal, point II.2, the Examining Division raised an objection under Article 123(2) EPC against amendment (9). This objection is not well founded.

The fact that the Examining Division admitted (see page 4, first paragraph) that Figure 3A shows a barrier layer 50, 60 filling the second contact holes 33, 34 and extending around these holes, indicates, in the Board's judgement, that the amendment is indeed admissible. Notwithstanding the disclosure of Figure 3A, the Examining Division, however, came to the conclusion that feature (9) goes beyond the content of the application as filed in view of the fact that there is not sufficient disclosure in terms of **structure and function** of this feature which is meant to define an

inventive merit over the prior art, in particular as regards the alleged improved adhesion of the barrier layer to the underlying layer. In support of its conclusion, the Examining Division cited decision T 241/88. In this decision the Board emphasised that, in accordance with the earlier decision T 169/83 (OJ EPO 1985, 193), in order for features contained in the drawings to be included in the claims "the condition must be satisfied that the features are clearly shown in the drawings originally filed and are clearly, unmistakably and fully derivable from the drawings in terms of structure and function by a person skilled in the art to enable him to recognise these features as forming part of the invention when considering the content of the description as a whole" (see point 2.2, second paragraph, of the reasons). In the present case, these conditions are met. Indeed, feature (9) is clearly shown in the original Figures 3A and 4, as the Examining Division itself found (see above). Moreover, it is clear to the skilled person that the function of the barrier layer is to act as a physical barrier to prevent precipitation of silicon atoms from an Al-Si metallization film at an ohmic contact with a silicon substrate (see the application, page 5, lines 3 to 12). In order for this function to be fulfilled, the barrier layer should be formed both in the contact hole and around the periphery thereof, as shown in Figures 3A and 4. It is undisputed that no indication is given in the application as filed that feature (9) also improves the adhesion of the barrier layer to the underlying silicon substrate. This is, however, a secondary effect achieved by the invention, irrelevant for the assessment of the admissibility of the amendment under Article 123(2) EPC. In fact, even without being aware

of such an effect, the skilled person would be able to recognise feature (9) as forming part of the invention when considering the content of the description as a whole, the invention concerning the use of the metallization film provided in the memory cell portion in order to form a barrier layer with respect to the Al-Si metallization film provided in the peripheral portion of the semiconductor memory device.

2.3 A further objection under Article 123(2) EPC, raised by the Examining Division, was that, although the amendments concerning the definition of the first and second insulation films have their basis in the embodiments of Figures 3A and 3B, "these amendments have been taken out of their proper context of essential features which are explicitly discussed in the description" (see the decision under appeal, point II.2, page 4, second paragraph). In the Board's judgement, this objection is not well founded either. Pursuant to Article 84 EPC the claims shall define the matter for which protection is sought. This matter is defined in terms of the technical features of the invention (Rule 29(1), first sentence, EPC). In particular, the claim has to state the essential features of the invention (Rule 29(3) EPC), whereby "essential features" means that they solve the technical problem underlying the invention (Rule 27(1)(c) EPC). For the purpose of Article 123(2) EPC, the content of the application as filed includes the drawings, so that features which are contained in the drawings may be used to amend the claims provided the condition defined in the case law of the Boards of Appeal and referred to in point 2.2 above is met. In this respect, a distinction should be drawn between the

context of a specific embodiment and that of the invention as claimed, which represents the solution to the stated technical problem. In the Board's judgement, a specific feature which is disclosed in a drawing in the context of a particular embodiment of the invention and which is recognised by the skilled person as being essential to the performance of the invention, in other words necessary for the solution of the problem to which the invention relates, may well be included in a claim without having to introduce any other feature of the particular embodiment in which the specific feature is framed. Whether the other features are required for the object of the embodiment to function is not relevant, because, as stated above, the invention as claimed must only define those features which solve the technical problem. It is not the aim of Article 123(2) EPC to oblige the applicant or the patentee to unduly restrict the extent of protection conferred by a claim by including into the claim features of a drawing (an embodiment) which do not contribute to the solution of the problem.

In the present case, only one preferred embodiment of the invention is represented in Figures 2 to 4. All the amendments of claim 1 have a basis in the application as filed and concern essential features of the invention. Moreover, in the Board's judgement, there is no need to introduce any other feature in the amended claim 1.

2.4 Claims 2 to 6 essentially correspond to the original claims 3, and 5 to 8. The subject-matter of claim 7 is disclosed in the application as filed, Figures 2 to 4, page 8, lines 3 to 35, page 12, lines 5 to 19, and

page 4, lines 23 to 25.

2.5 The description has been brought into conformity with the amended claims.

2.6 For these reasons, the application meets the requirements of Article 123(2) EPC.

3. *Article 84 EPC*

There are no objections under Article 84 EPC.

4. *Article 54 EPC*

4.1 Document D1 concerns a semiconductor memory device as recited in the preamble of claim 1 (see Figure 2). According to Section II, "low resistive $TaSi_2$ on polysilicon is implemented as the gate electrode material." Moreover, "this polycide layer is also used to realize low resistive bit lines" of the memory cells (see Figure 1). In Section VII, it is stated that "high-speed performance was obtained by the extensive use of $TaSi_2$ on source, drain and gate of most NMOS transistors in periphery circuits, on bit lines and also as low resistive interconnects beneath Al lines." This statement in Section VII would not make any technical sense, if the bit lines are considered to be made of polycide according to Section II. In view of the fact that bit lines are conventionally made of doped polysilicon, the expression "bit line" in Section VII can, however, be interpreted as referring to such a conventional polysilicon bit line. Thus, D1 discloses, on the one hand, that in DRAM devices bit lines are used, which are made of a metal silicide film on a

polysilicon film, this technical development being acknowledged in the present application on page 5, lines 26 to 31, and page 6, lines 20 to 24, and, on the other hand, that $TaSi_2$, and not polycide, is used as low resistive interconnects beneath Al lines. Hence, there is no mention in D1 that the first metallization film in the memory cell portion, including a refractory metal silicide film on a polysilicon film, further constitutes a barrier layer in the peripheral circuit portion, as specified in the characterising part of claim 1.

4.2 Document D2 (see abstract) addresses the same problem underlying the present application, namely Si precipitation at the contact between Al-Si metallization and silicon. The solution consists in the provision of a thin $TaSi_x$ ($x<2$) layer underneath the aluminium-based metallization, which acts as a barrier against silicon precipitation. Attention is also drawn to a statement on page 258, according to which most silicides with low contact resistance react with the top aluminium metallization and thus must be separated from aluminium by an additional diffusion layer. Thus, also D2 does not disclose the feature of claim 1 that the first metallization film in the memory cell portion, including a refractory metal silicide film on a polysilicon film, further constitutes a barrier layer in the peripheral circuit portion.

4.3 For these reasons, the subject-matter of claim 1 is novel, having regard to documents D1 and D2.

5. *Inventive step*

5.1 An essential feature of the present invention as claimed consists in that the peripheral circuit portion of the semiconductor memory device contains contact holes having a barrier layer formed therein and around a periphery thereof, this barrier layer being constituted by the same metallization film which is used for bit lines in the memory cell portion and has a dual-layer stacked structure of a polysilicon layer and a metal silicide layer. Thus, the invention is based on the idea of providing a barrier layer made of the same polycide structure which is used for bit lines, i.e. with a different function, in a different region of the device. This is possible because the peripheral circuit portion does not employ bit lines. The above idea is not obvious to a skilled person, having regard to the cited documents.

Both D1 and D2 teach away from the present invention. Indeed, as shown above (see points 4.1 and 4.2), their teaching is the use of a single layer of metal silicide as a barrier layer, in particular $TaSi_2$ according to D1 and $TaSi_x$ according to D2. Document D2 also envisages the possibility of a double layer to solve the same problem as the present invention, i.e. silicon diffusion at the contacts of the Al-Si metallization with shallow diffusion regions in silicon. However, such double layer is different from the claimed polycide structure because it comprises a metal silicide and a diffusion barrier between the silicide and the top aluminium metallization.

Moreover, there would be no reason for the skilled person to think that the polycide structure used for bit lines would also be suitable for making a barrier layer, bearing in mind that bit lines must provide good conduction of charge to and from memory cells whereas barrier layers have to prevent diffusion between adjacent layers. Indeed, these requirements are quite different, so that the skilled person would not consider that the bit line structure could provide a more effective barrier layer.

5.2 The Examining Division's argumentation concerning inventive step (see point II.5.1 of the decision under appeal) is based on the allegation that "D1 teaches the skilled person that the silicide layer of the polycide metallization film is necessary for forming a barrier between silicon and an aluminium based metallization." As a matter of fact, the structure of the peripheral circuits is not disclosed in document D1. It is only stated that the material $TaSi_2$ can be used for bit lines and also as low resistive interconnects beneath Al lines. This disclosure is, however, not sufficient for alleging that "the silicide layer which is used in the polycide film of the bit lines ... has also to be used in the same level of metallization also in the contact hole structures of the peripheral circuit portion", as the Examining Division does. It thus appears that the Examining Division interprets the insufficient disclosure of a prior art document with foreknowledge of the invention with the consequence that an *ex post facto* analysis results.

5.3 For these reasons, the subject-matter of Claim 1 involves an inventive step, having regard to documents

D1 and D2.

6. Since the application and the invention to which it relates meet the requirements of the EPC, a European patent can be granted.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the following documents:

Claims: No. 1-7 as filed with the letter of 26 November 1998,

Description: Pages 1,5-7,9-12 as originally filed,
Page 2,3 as filed with the letter of 26 November 1998,
Page 4,8 as filed with the letter of 12 July 1994,

Drawings: Sheets 1/3-3/3 as originally filed.

The Registrar: The Chairman:

M. Beer G. Davies