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D E C I S I O N
of 17 December 1997

Case Number: T 0810/94 - 3.4.1

Application Number: 88108435.4

Publication Number: 0292972

IPC: H01L 21/76

Language of the proceedings: EN

Title of invention:
IC with recombination layer and guard ring separating VDMOS and CMOS or the like

Applicant:
NISSAN MOTOR CO., LTD.

Opponent:
-

Headword:
Recombination layer/NISSAN MOTOR CO. LTD.

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes)"
"No suggestion in the prior art of the problem addressed by the invention"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0810/94 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 17 December 1997

Appellant: NISSAN MOTOR CO., LTD.
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Representative: Grünecker, Kinkeldey,
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 11 May 1994 refusing European patent application No. 88 108 435.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. Davies
Members: R. K. Shukla
U. G. O. Himmler

Summary of Facts and Submissions

I. European patent application No. 88 108 435.4 relating to an integrated circuit device with a recombination layer and a guard ring separating a VDMOS from other circuit components was refused by a decision of the Examining Division, dated 11 May 1994, on the ground that claims 1 to 10 as filed with the letter dated 26 April 1993 did not involve an inventive step within the meaning of Article 56 EPC, having regard to the following prior art documents:

D1: EP-A-0 176 747
D2: FR-A-2 320 636.

II. The applicant lodged an appeal on 18 July 1994, paying the appeal fee the same day, and filed a new set of claims and an amended page of the description with the statement of the grounds of appeal on 21 September 1994. As an auxiliary request, the applicant requested that oral proceedings should be appointed.

In relation to claim 1 forming the basis of the contested decision, new claim 1 was amended so that it was in a two-part form according to Rule 29(1) EPC taking into account the prior art as disclosed in document D1.

III. In a communication annexed to a summons to oral proceedings, the Board informed the applicant of its provisional view that the semiconductor device forming the subject-matter of claim 1 did not appear to involve an inventive step having regard to the above-cited prior art documents. Also, the following prior art document representing the common general knowledge in

the art was cited by the Board in respect of dependent claims 3 and 4 in support of the Board's submission that it was well known that doped or undoped polycrystalline silicon provides carrier traps at the grain boundaries:

D3: SEMICONDUCTOR DEVICES- Physics and Technology by S. M. Sze, 1985, page 364, second paragraph.

IV. In response to the above communication, the applicant filed two sets of claims forming respectively the basis of its main request and an auxiliary request, and new page 1 of the description.

V. At the oral proceedings held on 17 December 1997, the above sets of claims were withdrawn, and the applicant requested the grant of a patent on the following application documents:

Description: pages 1, 1a to 15 as filed during the oral proceedings on 17 December 1997;

Claims: 1 to 11 as filed during the oral proceedings on 17 December 1997;

Drawings: Sheets 1/6 to 6/6 as originally filed.

VI. Claim 1 of the above request has the following wording:

"A semiconductor device comprising:
a highly doped lower layer (1) of a first conductivity type (n-type), formed in a semiconductor substrate body;
a lightly doped upper layer (2) of said first conductivity type, formed on top of said highly doped lower layer within said semiconductor substrate body;
a vertical MOSFET (10) formed in a first portion (2a) of said lightly doped upper layer so that said lightly

doped layer is substantially used as a drain region of said vertical MOSFET;
a second circuit component (20,30) formed in a second portion (2b) of said lightly doped upper layer;
a guard ring (33, 37, 38) formed in said lightly doped upper layer so as to separate said first and second portions (2a, 2b); and
a component interference preventive layer (35,36) formed between said highly doped lower layer (1) and at least said portion (2b) of said lightly doped upper layer (2), said guard ring (33, 37, 38) being formed so as to reach said component interference preventive layer (35, 36),
characterised in that
said component interference preventative layer is a recombination layer (35,36) for facilitating recombination of minority carriers in the lightly doped upper layer of the first conductivity type, said recombination layer being a doped polycrystalline semiconductor layer of said first conductivity type."

VII. The applicant made essentially the following submissions:

(i) In the prior art document D1, electrical components are electrically isolated from each other by the provision of (a) an insulating layer surrounding a component, (b) a reversed biased PN junction, or (c) an insulating layer and a reverse biased PN junction. In contrast to the above, in the present invention a recombination layer for the recombination of minority carriers is provided between a highly doped lower layer and a portion of a lightly doped upper layer, whereby the minority carriers which are injected from a source region of a VDMOS are prevented from reaching the electrical component enclosed by the guard ring and the

recombination layer in the lightly doped upper layer. Contrary to the statement made by the Examining Division in the decision under appeal, a recombination layer is not equivalent to an insulating layer or a reverse biased junction which blocks both types of charge carriers, whereas a recombination layer for minority carriers is a good conductor for the majority carriers.

(ii) Although fly-wheel currents are known in an electrical circuit such as shown in Figure 8 of the application in suit, it was not known in the art that the fly-wheel current would cause injection of minority carriers from the source region of the VDMOS in the drain region. Since the prior art documents and, in particular, document D1 does not address the problem of electrical interference caused by minority carriers in a semiconductor device containing a VDMOS, there was no reason for a skilled person to replace the insulating layer in the device of Figure 9A of document D1 with a recombination layer.

(iii) Document D2 teaches to provide a recombination region within the base region of a vertical parasitic bipolar transistor in order to reduce the gain of the transistor, so that the provision of a recombination layer at the boundary between the highly doped lower layer and the lightly doped upper layer as in the claimed invention is not suggested by this document. Moreover, the effect of the minority current injection due to the fly-wheel current is not discussed in document D2, and it cannot be derived from this document that the latch-up of the CMOS device caused by the fly-wheel

current is comparable to the problem of parasitic bipolar transistor in a CMOS, addressed in document D2. Thus, a combination of the teachings of documents D1 and D2 would not lead to the claimed subject-matter.

Reasons for the Decision

1. *Amendments*

Claim 1 has been amended so that it incorporates the subject-matters of original claims 3 and 4, with the exception that, whereas original claims 3 and 4 specify that the recombination layer is a doped polycrystalline ***silicon*** layer, doped with an impurity of first conductivity type, the amended claim 1 states that the recombination layer is a doped ***semiconductor*** layer of first conductivity type (emphasis added by the Board).

In the Board's view, the above generalisation from a "silicon layer" to a "semiconductor layer" does not go beyond the content of the application as filed, since according to claim 2 as originally filed, the recombination layer is "made of a ***material*** capable of promoting recombination of carriers ". Thus, it is apparent that the application as filed sought protection for any such material including a doped polycrystalline semiconductor material.

Other amendments to the claims are of an editorial nature. The description has been amended so as to be consistent with the new claims.

The amendments thus meet the requirements of Article 123(2) EPC.

2. *Inventive step*

The only issue in the present appeal is that of inventive step.

2.1 The prior art coming closest to the claimed invention is disclosed in document D1. In the semiconductor device described with reference to Figure 9A of this document, a vertical MOSFET (49) and a CMOS (46,47) are formed in a semiconductor substrate comprising a lightly doped upper layer (48) and a highly doped lower layer (21), the CMOS being isolated from the vertical MOSFET by an insulating layer (23) formed at the interface of the lower and upper layers and an insulating layer (37) surrounding the CMOS and contacting the insulating layer (23) at the interface (see page 9, lines 9 to 29). Moreover, it follows from the description of the embodiment of Figure 8C (see page 9, lines 3 to 6), that instead of the insulating layer (37) surrounding the CMOS, a P-type diffusion ring (44) which contacts the insulating layer (23) can be provided.

The semiconductor device according to claim 1 is thus distinguished from the above prior art in that, instead of an insulating layer (23) at the interface, a recombination layer (35,37) for the minority carriers is provided at the interface of the upper and lower layers, the recombination layer being a doped polycrystalline semiconductor layer having the same conductivity type as the upper and lower layers.

2.2 In the application in suit, conventional integrated circuits containing a vertical MOSFET and a CMOS are discussed with reference to Figures 6 to 9 (see column 1, line 30 to column 3, line 27 of the published application). It follows from this discussion that

under certain transient conditions which prevail when the current supplied to an inductive load is switched off, a relatively large transient current e.g. a flywheel current, flows through the vertical MOSFET which is in the turned- off state. The provision of a recombination layer for minority carriers in combination with a guard ring according the present invention prevents the fly-wheel current from reaching the CMOS and thereby prevents its latch-up.

2.3 In connection with the above-mentioned conventional devices, and in particular in the circuit arrangement of Figure 8, it was contended by the applicant that, although a skilled person might reasonably expect transient currents to be produced when the current to an inductive load, such as a motor, is switched off, it was not known that in the conventional devices such a transient current would inject minority carriers through a P- well region (3) of the vertical MOSFET into the drain region (i.e. the upper lightly doped layer). The inventors of the application in suit realised that such a transient current in the vertical MOSFET would inject minority carriers causing the latch-up of the CMOS. The Board follows the above submissions, so that, in the Board's view, it cannot be derived from the discussion of the above-mentioned conventional devices in the application in suit that it was known in the art that the CMOS devices needed to be isolated from minority carriers which are injected from a vertical MOSFET during transient conditions.

2.4 With regard to document D1, the Board agrees with the submissions made by the applicant (see paragraph VII(i)) that the document is exclusively concerned with electrically isolating a device region (40) containing semiconductor element(s) from other semiconductor elements formed in the rest of the substrate, and that this is achieved by using insulating layers alone or

using an insulating layer in combination with a reverse-biased PN junction (see Figures 8A to 8C; page 1, lines 1 to 25; page 3, lines 29 to 33). Also, silicon dioxide, silicon nitride and undoped polycrystalline silicon are disclosed as the materials for the insulating layer (see, e.g. page 6, lines 17 to 21; page 8, line 35 to page 6, line 3). It therefore follows that the device region (40) is completely electrically isolated irrespective of whether the charge carriers are electrons or holes, from the other semiconductor elements. An electrically insulating layer or a reverse-biased PN junction having a charge-depleted zone, contrary to the assertion of the Examining Division, is thus not electrically equivalent to a recombination layer which provides deep level traps only for the minority carriers (holes in the N-type drain region of the present invention). Moreover, in document D1 the problem caused during the transient state of an integrated circuit is not addressed. In particular, it is not derivable that during the transient state, minority carriers are injected from the vertical MOSFET into the drain region.

2.5 Document D2' is concerned with controlling the minority carrier lifetime of transistors both to improve the speed of operation or to reduce the gain. In CMOS devices described with reference to Figures 2 and 3 of this document (see, column 3, line 66 to column 4, line 9), a recombination region (22, 24) is provided beneath the source and drain regions (15 and 16) to reduce the gain of the vertical parasitic bipolar transistor. In the bipolar transistors described with reference to Figures 4 and 5 on the other hand, a recombination region (44,46) for controlling the minority carrier lifetime is provided mainly in the collector region (38) to increase the speed of operation of the bipolar transistor (see, column 4, lines 38 to 47).

Thus, in the Board's view, a skilled person learns from document D2', that the provision of a recombination layer at an appropriate location in a device can provide traps for minority carriers and thereby reduce their lifetime. Document D2', however, does not address the problem of minority carriers during the transient state in a device such as known from Figure 9A of document D1 including a vertical MOSFET.

2.6 From the foregoing, it is evident that the cited prior art does not provide any hint regarding the problem of injection of minority carriers occurring during the transient state in an integrated circuit device such as known from document D1. Consequently, even if a skilled person contemplated other means for isolating the device region (40) in document D1, he had no reason to depart from the teaching of this document and provide a recombination layer for the minority carriers.

2.7 For the foregoing reasons, in the Board's judgement, the subject-matter of claim 1 involves an inventive step within the meaning of Article 56 EPC.

Claims 2 to 11 are dependent on claim 1, and are therefore allowable.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the application documents mentioned in paragraph V above.

The Registrar: The Chairman:

M. Beer G. Davies