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D E C I S I O N
of 20 November 1997

Case Number: T 0866/94 - 3.4.1

Application Number: 90110524.7

Publication Number: 0405183

IPC: H01L 21/76

Language of the proceedings: EN

Title of invention:
Dielectric isolation used in high voltage power IC process

Applicant:
NATIONAL SEMICONDUCTOR CORPORATION

Opponent:
-

Headword:
Dielectric isolation/NATIONAL SEMICONDUCTOR CORP.

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - no"
"Obvious selection from a limited number of available methods"

Decisions cited:
-

Catchword:
-

Case Number: T 0866/94 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 20 November 1997

Appellant:

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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted on 20 June 1994 refusing European patent application No. 90 110 524.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. Davies
Members: R. K. Shukla
U. G. O. Himmler

Summary of Facts and Submissions

I. European patent application No. 90 110 524.7 relating to a process for forming high voltage transistors in an oxide-isolated semiconductor wafer was refused by a decision of the Examining Division, dated 20 June 1994, on the ground that claim 1 as originally filed did not involve an inventive step within the meaning of Article 56 EPC, having regard to the following prior art documents:

D1 - Proceedings of the IEEE 1987 Custom Integrated Circuits Conference, May 4 to 7, 1987; Portland, Oregon; "Dielectrically Isolated Intelligent Power Switch", pages 443 to 446;

D3 - Proceedings of the 19th Annual IEEE Power Electronics Specialists Conference, April 11 to 14, 1988; Kyoto, Japan; "High Voltage, New Driver IC Technique based on Silicon Wafer Direct-Bonding (SDB)", pages 1325 to 1329 ; and

D7 - EP-A-0 118 921.

II. The applicant lodged an appeal on 17 August 1994, paying the appeal fee the same day, and filed a new set of claims 1 to 6, a supplementary portion of the description, and Figures 1 to 7, with the statement of the grounds of appeal on 20 October 1994.

In relation to claim 1 forming the basis of the contested decision, new claim 1 has been amended so that it is in a two-part form according to Rule 29(1) EPC, and additionally contains reference signs in accordance with Rule 29(7) EPC. The new claim 1 has the following wording:

" A process for forming high voltage transistors in a semiconductor wafer which will include low voltage conventional transistors, said process including the steps:

(a) starting with a first wafer (10) of semiconductor material having a resistivity suitable for the fabrication of said low voltage transistors and a second wafer (12) of semiconductor material having a resistivity that is substantially lower than that of said first wafer,

(b) polishing a face of said first wafer and of said second wafer to produce flat mirror finishes thereon,

(c) forming an oxide (11, 14) on each wafer on said polished faces,

(d) washing said oxide coated wafer faces to render them hydrophilic,

(e) placing said hydrophilic faces together to produce adhesion between said first and second wafers while leaving exposed an opposite face of each of said wafers,

(f) heating said adhered wafers to coalesce said oxide coatings thereby to join said first and second wafers into a unitary structure,

(g) grinding and etching said exposed face of said first wafer until a predetermined thickness (10') thereof remains,

(h) etching a groove (17) in said first wafer that extends through it and through said oxide (15) that joins said wafers together to expose a portion of said second wafer semiconductor material,

(i) backfilling said groove with epitaxially deposited semiconductor material,

(j) shaping the exposed surface of said first wafer for subsequent planar processing, and

(k) forming a high voltage transistor in said backfilled semiconductor material,

characterised in that after step (a) and prior to step (b), at least one epitaxial layer (13) of semiconductor material is formed on one face of said second wafer, that it is said one face of said second layer which is polished and oxidised, and that said groove extends into said epitaxial layer."

III. In a communication annexed to a summons to oral proceedings, the Board informed the applicant of its provisional view that the process for forming high voltage transistors forming the subject-matter of claim 1 did not appear to involve an inventive step having regard to the above cited prior art documents.

No amendments were filed by the applicant in response to the above communication. The applicant thus requests that the decision under appeal be set aside and that a patent be granted on the basis of the following text and drawings:

Description: pages 1 to 3 and 5 to 9 as originally filed;
page 4 including amendments as filed with the letter dated 20 October 1994;

Claims: 1 to 6 as filed with the letter dated 20 October 1994; and

Drawings: Figures 1 to 7 as filed with the letter dated 20 October, 1994.

IV. The applicant's arguments in support of the above request can be summarised as follows:

In contrast to the process disclosed in the closest prior art document D1, in the process according to the present invention, at least one epitaxial layer is

formed on one face of a second wafer, and the exposed face of the epitaxial layer is polished and then oxidised prior to joining the two wafers together. Moreover, the groove specified in step (h) of the claimed process extends into the epitaxial layer. The provision of an additional epitaxial layer provides flexibility in that a wide variety of high voltage devices can be combined with a variety of low voltage devices, as disclosed in the application as published at column 6, lines 26 to 30.

In the dielectric isolation based on direct bonding of silicon wafers, disclosed in section 2. "Dielectric Isolation by Silicon Wafer Direct-Bonding" of document D3, wafer (2), corresponding to the second wafer of claim 1 of the application in suit, has a higher resistivity than the first wafer (1), is not provided with an epitaxial layer and is neither polished nor oxidised before it is bonded to the oxidised first wafer (1). The process according to document D3, thus, does not disclose some of the features of paragraphs (a), (b), (c), and (d), and the features of the characterising part of the claim. Moreover, in document D3, there is only a brief reference to the device shown in Figure 8, and there is no disclosure in the document that the N^- type layer in the VDMOS is an epitaxial layer formed on N^+ drain.

Document D7 does not concern formation of low and high voltage transistors in a common semiconductor wafer, as does the present invention. The formation of an N^- epitaxial layer on an N^+ drain layer is mentioned in this document as an example only, and not as a well-accepted practice in the art. This document therefore does not suggest the formation of an epitaxial layer on a second wafer in the process disclosed in document D1. The fact that in the decision under appeal three documents, i.e. D1, D3 and D7, are required for the

assessment of inventive step, suggests that the subject-matter of claim 1 was not obvious to a person skilled in the art.

Reasons for the Decision

1. The appeal is admissible.

2. *Inventive step*

The only issue in the present appeal is that of inventive step of the subject-matter of claim 1.

2.1 The prior art coming closest to the invention is disclosed in document D1 acknowledged in the application in suit. It is not in dispute that a process for forming high voltage transistors in a wafer, as claimed in the precharacterising part of claim 1 is known from this document (see, section "IP-2 Process and the Device Structure", in particular, page 444, left-hand column, first two paragraphs and Figure 1; page 444, right-hand column, lines 1 to 5 and Figure 4).

The process according to claim 1 is thus distinguished over this closest prior art process only in that prior to the bonding of the wafers, (a) an epitaxial layer (13) is provided on the second wafer (12), (b) the epitaxial layer is then polished, and (c) the polished surface of the epitaxial layer is subsequently oxidised.

As a result of the above distinguishing features, in the device produced according to the invention an epitaxial layer (13) is sandwiched between the low resistivity second wafer and the regrown epitaxial

layer (19) in the high voltage section. In the device shown in Figure 4 produced according to the process of document D1, on the other hand, such an epitaxial layer is not provided in the high voltage section.

2.2 In connection with the above distinguishing features, it was submitted by the applicant that the epitaxial growth of layer (13) has the advantage over the IP-2 process described with reference to Figure 1 in document D1 in that the epitaxial growth affords the flexibility of combining a wide variety of high voltage devices with a variety of low voltage devices in a semiconductor wafer, as disclosed in the published application in suit in column 6, lines 26 to 30. The object of the invention of providing a high voltage device having a high breakdown voltage, stated in column 2, lines 16 to 21 of the published application, it was argued by the applicant, was in relation to a known device, i.e Intelligent Power-1 (IP-1) structure, mentioned in the introductory part of document D1 , and not in relation to the closest prior art process (IP-2 process) described therein with reference to Figure 1.

2.3 The Board agrees with the above submissions, so that the objective problem addressed by the claimed invention was to provide a process which was flexible, whereby a wide variety of high voltage devices could be combined with a variety of low voltage devices in a semiconductor wafer.

It is already known in the art to combine high and low voltage devices in a common semiconductor wafer (see, e.g. document D1, Figure 4; document D3, Figures 1 and 3), so that the need to provide a process which would combine various types of high voltage devices with low voltage devices would be obvious to the skilled person.

2.4 Document D3 describes a process for forming high voltage transistors in a wafer, based on Silicon wafer Direct Bonding (SIDB) technique as in document D1. In the technique described with reference to Figures 2a to 2c in Section 2 - "Dielectric Isolation by Silicon Wafer Direct-Bonding", the bulk resistivity of the P-conductivity type second wafer (2) is not lower than that of the first wafer (1), as required in paragraph (a) of claim 1. Also, the second wafer is not provided with an epitaxial layer as in the characterising part of the claimed process. Furthermore, as submitted by the applicant, the oxidised surface of the first wafer is directly bonded to the high resistivity second wafer.

However, in a variation of the technique for forming a VDMOS device combined with a BiCMOS logic as shown in Figure 8 (see page 1326, Section 4 - "Application for Present IC Techniques"), a relatively high resistivity layer (N^-) is provided between a low resistivity (N^+) drain region and a P region in the high voltage VDMOS, as in the application in suit. Although a process for producing the device of Figure 8 is not specifically described in document D3, in the Board's view, it follows from the location of the dielectric layer above the N- layer in the CMOS section of the device of Figure 8, that the N- layer has to be formed **in or on** the N+ wafer prior to bonding of the wafers together. There is no disclosure in the document as to how the N^- layer is formed. In the Board's view, however, and this was also the contention of the applicant, in the art of semiconductor device technology, there is a limited number of methods available for the formation of such a layer, i.e. counter doping by diffusion or ion implantation in the N+ wafer or formation of a relatively lightly N^- doped epitaxial layer on the N^+ wafer. Furthermore, a skilled person must be presumed to be aware of the general advantages and drawbacks of

each of the above methods, in particular, of the advantage afforded by the epitaxial growth of a semiconductor layer in controlling its thickness and impurity concentration, these being the parameters which are generally known to determine the device characteristics of high voltage devices. Moreover, as can be seen from the disclosure in document D7, in the formation of a high voltage device such as VDMOS, it is known to provide a high resistivity layer (12) on a low resistivity substrate (1) **by epitaxial growth** (see page 5, lines 3 to 7, page 2, lines 22 to 27; and Figures 2 and 3(a)). Thus, the formation of N^- layer in the device of Figure 8 of document D3 by epitaxial deposition represents an obvious selection from a limited number of methods available to the skilled person. Also, in view of the above, the provision of a high resistivity layer, such as the layer N^-, in the device shown in Figure 4 of document D1 by epitaxial deposition on an N+ wafer with a view to provide flexibility to the IP-2 process disclosed in document D1 was obvious to the skilled person. Moreover, in accordance with the IP-2 process disclosed in document D1, such a layer would have to be provided prior to the bonding of the two wafers.

2.5. For the foregoing reasons, in the Board's judgement, the subject-matter of claim 1 lacks an inventive step within the meaning of Article 56 EPC.

Dependent claims 2 to 6 are also not allowable because of their dependency on claim 1.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer G. Davies