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D E C I S I O N
of 21 October 1998

Case Number: T 0867/94 - 3.4.1

Application Number: 89312274.7

Publication Number: 0376479

IPC: H01L 21/3105

Language of the proceedings: EN

Title of invention:
Method for manufacturing a semiconductor device having a phospho silicate glass layer as an interlayer insulating layer

Applicant:
Kabushiki Kaisha Toshiba

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 123(2), 84, 56

Keyword:
"Main request: inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0867/94 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 21 October 1998

Appellant: Kabushiki Kaisha Toshiba
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Decision under appeal: Decision of the Examining Division of the European Patent Office posted 20 June 1994 refusing European patent application No. 89 312 274.7 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: G. Davies
Members: G. Assi
R. K. Shukla

Summary of Facts and Submissions

I. The appellant (applicant) lodged an appeal, received on 5 August 1994, against the decision of the Examining Division, dispatched on 20 June 1994, refusing the application No. 89 312 274.7 (publication No. 0 376 479). The fee for the appeal was paid on 9 August 1994. The statement setting out the grounds of appeal was received on 21 October 1994.

In the decision under appeal, the Examining Division held that the application did not meet the requirements of Articles 52(1) and 56 EPC, having regard to the following documents:

(D1) EP-A-0 155 699 (cited in the European search report) and

(D2) WO-A-86/01638 (cited according to the EPO Guidelines, C-VI, 8.9).

The decision under appeal further contains comments (see "Additional comments") which "do not form part of the reasons for the refusal of the application, but are added for completeness". In particular, these comments raised objections under Articles 123(2) and 84 EPC, against independent claims of the main request and the first auxiliary request before the Examining Division.

II. During the appeal proceedings, the Board introduced the following document cited in the European search report:

(D3) EP-A-0 081 226.

III. The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Main request:

Claims:

No. 1 to 7, 8 (page 14) as filed with the letter of 20 October 1994,

No. 8 (page 15) as filed with the letter of 16 July 1998,

Description:

Pages 1 to 3, 5, 7, 8 as originally filed,

Page 4, 6, 9, 10 as filed with the letter of 16 July 1998,

Drawings:

Figures 1A, 1B, 1C, 1D, 1E, 1F as filed with the letter of 22 February 1990,

Figures 2A, 2B, 2C, 2D, 2E, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 6A, 6B, 6C as originally filed,

Auxiliary request:

Claims:

No. 1 to 8 as filed with letter of 20 October 1994,

Description:

Pages 1 to 3, 5 to 10 as originally filed,

Page 4 as filed with letter of 20 October 1994,

Drawings:

Figures 1A, 1B, 1C, 1D, 1E, 1F as filed with letter of 22 February 1990,

Figures 2A, 2B, 2C, 2D, 2E, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 6A, 6B, 6C as originally filed.

Furthermore, the appellant requested that oral proceedings be held in the event that the above mentioned requests are not granted.

IV. The wording of Claim 1 according to the main request reads as follows:

"1. A method for forming a multilevel interconnection structure on a substrate (30) having a main surface, the method comprising the steps of:
forming an insulating layer (31) on the main surface of the semiconductor substrate (30);
depositing a polysilicon layer (32) on the insulating layer;
depositing a refractory metal silicide layer (33) on the polysilicon layer (32);
selectively removing the polysilicon layer (32) and the refractory metal silicide layer (33);
depositing an oxide layer (35) on the polysilicon layer (32) and refractory metal silicide layer (33) without an intermediate step of thermal oxidation of the refractory metal silicide layer (33) being performed between the step of forming the polysilicon layer (32) and refractory metal silicide layer (33) and the step of depositing the oxide layer (35);
depositing a first layer (36) of phospho silicate glass (PSG) or boron-doped phospho silicate glass (BPSG) on the oxide layer (35);
after depositing the first PSG or BPSG layer (36), heating the substrate in steam to perform a smoothening of the first PSG or BPSG layer (36) and cause oxidization of the refractory metal silicide layer (33); and
forming a wiring layer (37) on the PSG or BPSG layer (36)."

The wording of Claim 6 according to the main request reads as follows:

"6. A method for manufacturing a semiconductor device having a multilevel interconnection construction on a semiconductor substrate (30) having a main surface, the method comprising the steps of:
forming a first wiring layer (32, 33) comprising a refractory metal silicide on the main surface of the substrate (30);
depositing an oxide layer (35) covering the first wiring layer (32, 33) without an intermediate step of thermal oxidation of said first wiring layer (32, 33) being performed between the step of forming the first wiring layer (32, 33) and depositing the oxide layer (35);
depositing a first layer (36) of phospho silicate glass (PSG) or boron-doped phospho silicate glass (BPSG) on the insulating layer (35);
after depositing the first PSG or BPSG layer (36), heating the substrate in steam to perform a smoothening of the first PSG or BPSG layer (36) and oxidization of the first wiring layer (32, 33);
forming a second PSG or BPSG layer (40) on the smoothened first PSG or BPSG layer (36);
heating the semiconductor substrate in an ambient to which phosphorus has been added;
removing the second PSG or BPSG layer (40) and forming a second wiring layer (37) on the smoothened first PSG or BPSG layer (36)."

The wording of Claim 8 according to the main request reads as follows:

"8. A method for manufacturing a semiconductor device having a multilevel interconnection construction on a semiconductor substrate (30) having a main surface, the method comprising the steps of:
forming a first wiring layer (32, 33) comprising a refractory metal silicide on the main surface of the substrate (30);
depositing an oxide layer (35) covering the first wiring layer (32, 33) without an intermediate step of thermal oxidation of the first wiring layer (32, 33) being performed between the step of forming the first wiring layer (32, 33) and depositing the oxide layer (35);
depositing a first boron-doped phospho silicate glass (BSPG) layer (36) on the insulating layer (35);
after depositing the first PSG or BPSG layer (36);
heating the substrate in steam to cause oxidation of the first wiring layer (32, 33) and smoothening the first BPSG layer (36);
forming a second BPSG layer (70) on the smoothened first BPSG layer (36);
forming a phospho silicate glass (PSG) layer (71) on the second BPSG layer (70);
heating the semiconductor substrate in an ambient to which phosphorus has been added;
removing the PSG layer (71); and
forming a second wiring layer (72) on the second BPSG layer."

In the above wording, the acronym "BSPG" should be "BPSG".

Claims 2 to 5 and 7 according to the main request are dependent claims.

V. The appellant argued essentially as follows:

The present invention concerns the formation of a multilevel interconnection structure in which the resistivity of the lower wiring comprising a refractory metal silicide layer is reduced without using an unreliable technique like thermal oxidation. The invention relies on the fact that the thermal treatment in the presence of steam involved in the reflow step causes oxidation of the metal silicide which is, by this stage, protected by both an oxide layer and a glass layer. In this way, since the silicide is not exposed to any oxidising medium, the resistivity can be accurately controlled. The combination of the resistivity control step and glass reflow process into a single step is neither disclosed nor suggested in the cited prior art. In particular, both D1 and D2 disclose exposing the lower wiring to an oxidising ambient, which method does not enable an accurate control of resistivity.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 The Board is satisfied that the amendments proposed in the main request meet the requirements of Article 123(2) EPC.

On page 16 of the decision under appeal, point 2.0, second paragraph, the Examining Division draws attention to the fact that there is no support in the original application for the general feature - contained in present Claims 1, 6 and 8 - that the oxide layer is deposited without thermal oxidation of the first (lower) wiring layer.

According to the appealed decision, this objection is not a ground on which the refusal of the application is based. However, the Board considers it useful to remark that the objection is not justified. In particular, the Examining Division points out that, according to the original disclosure, page 5, lines 25 to 26, an oxide layer is formed by a **CVD** process. During a following heat treatment in steam, the polysilicon layer and the molybdenum silicide layer (forming the first wiring) are oxidized to form a further oxide layer. The Board agrees that the above-quoted passage refers to a specific embodiment, whereas the claims are general and cover any method of deposition. However, the

combination of original Claims 1 and 2 provides a method in which an oxide layer is deposited (not necessarily by CVD) on the first wiring layer and a further oxide layer is formed by a following reflow heating in steam.

2.2 The Board is also satisfied that the amendments proposed in the main request meet the requirements of Article 84 EPC.

In this respect, the Board would like to comment on a feature of the claims to which the Examining Division drew attention on page 17 of the decision under appeal, point 3.0. The feature concerned - contained in present Claims 1, 6 and 8 - is that oxidation of the refractory metal silicide layer is caused during the reflow step of the glass layer covering said silicide layer. In the described embodiments, molybdenum silicide is used as the refractory metal silicide. However, according to the original description, page 9, lines 18 to 21, tungsten silicide and tantalum silicide may also be used in place of molybdenum silicide. The Examining Division thus held that it is not clear whether the claimed method is indeed successful with silicides other than molybdenum silicide, considering the complexity of the oxidation process, in particular the many factors on which it depends.

In the Board's judgement, however, the sentence on page 9, lines 18 to 21, should be interpreted in a different way, in particular as meaning that the applicant has (experimentally) found that tungsten silicide and tantalum silicide provide the same results as molybdenum silicide. The objection under Article 84 EPC is thus unjustified.

2.3 Novelty is not disputed. Thus, the only issue to be discussed is that of inventive step.

The present invention (see page 1, first sentence) refers to a method for manufacturing a semiconductor device having a multilevel interconnection construction on a substrate.

The method disclosed in Figures 1A to 1F of the present application (alternatively, the method disclosed in D1 - see below) is considered to represent the most pertinent state of the art. It comprises the following steps:

(a) forming an insulating layer on the main surface of the semiconductor substrate (see Figure 1A);

(b) depositing a polysilicon layer on the insulating layer (see Figure 1A);

(c) depositing a refractory metal silicide layer on the polysilicon layer (see Figure 1A);

(d) selectively removing the polysilicon layer and the refractory metal silicide layer (see Figure 1A);

(e) forming a first oxide layer by exposing the polysilicon layer and the refractory metal silicide layer to an oxidising ambient (see Figure 1B);

(f) CVD depositing a second oxide layer (see Figure 1B);

(g) depositing a layer of BPSG on the second oxide layer and thereafter a layer of PSG (see Figure 1C);

(h) after depositing the PSG layer, heating the substrate to perform a smoothening of the BPSG and PSG layers (see Figure 1D);

(i) removing the PSG layer (see Figure 1E);

(l) forming a wiring layer on the BPSG layer (see Figure 1F).

The method according to Claim 1 differs from the known one in that no thermal oxidation (see step (e)) is performed between the steps (c), (d) of selectively forming the polysilicon layer and refractory metal silicide layer and the step (f) of depositing the second oxide layer. The same difference exists with regard to the methods according to Claim 6 and Claim 8.

As already stated above, D1 could also be considered as the most pertinent state of the art. Indeed, this document discloses a method which essentially comprises the steps of the method shown in Figures 1A to 1F with the difference that a refractory metal silicide layer is not deposited on the polysilicon layer. In the following discussion, however, the method of Figures 1A to 1F is used as the starting point for the assessment of inventive step.

In the known process, the oxidation process (e) of the lower wiring layer comprising a refractory metal silicide layer and the heat treatment (h) for the

reflow process are performed separately. Thus, the manufacturing time is long. Moreover, exposing the refractory metal silicide layer directly to an oxidizing ambient causes difficulties in controlling resistivity of the silicide layer. The technical problem to be solved is, therefore, shortening the manufacturing time as well as controlling resistivity of the lower wiring layer without using unreliable techniques like thermal oxidation (see the application, page 3, lines 13 to 24, and letter of 20 October 1994, grounds of appeal, page 1, fourth paragraph).

The solution to the problem consists in omitting the thermal oxidation step, oxidation of the lower wiring layer nevertheless occurring during reflow of the glass layer, this solution being common to all independent Claims 1, 6 and 8 (see the features "depositing an oxide layer ... without an intermediate step of thermal oxidation of ..." and "heating the substrate in steam to ... oxidization of the ..."). Indeed, the omission of a step shortens the manufacturing time. Moreover, since the lower wiring layer is not any more exposed to an oxidising medium, accurate control of the resistivity is possible.

Achieving oxidation of the lower wiring layer covered by a glass layer during reflow of the glass layer, without a thermal oxidation step, is not suggested in the prior art.

In particular, in the known method disclosed in Figures 1A to 1F of the present application, a thermal oxidation step is necessary to control the resistivity of the lower wiring layer (see the present application, page 2, lines 3 to 9, page 3, lines 13 to 24, Figure 1B, 1D, and D1, page 8, line 5, to page 9, line 6, Figures 2A, 2B).

Document D1 (see Figures 2A to 2D) discloses a semiconductor device having a multi-layer wiring arrangement 23,24 mounted on a substrate. This wiring is surrounded by oxide films 28,27, whereby the first oxide film is formed by thermal oxidation. A BPSG layer 25 is deposited and heat treated in a steam atmosphere to form a smooth surface. Thereafter, a PSG film 37 is formed. Contact holes 39 are then etched and a polycrystalline silicon film 29 and an aluminium layer 31,33 are deposited. Thus, D1 teaches the need of a thermal oxidation step of the lower wiring formed of polysilicon (see page 8, lines 12, 17 and 18).

D2 discloses a semiconductor integrated circuit in which gate electrodes are formed of multi-layers of polysilicon and tantalum silicide. After formation of these electrodes, the circuit is thermally oxidised so as to form a protective oxide layer 25 over the exposed portions of the substrate and the gate electrodes (see page 4, lines 28 to 33). A glass layer 19 is then deposited and annealed. Thereafter, a polysilicon contact layer 20 and a patterned aluminium layer 41 are formed. Therefore, document D2 teaches the need of a thermal oxidation step of the gate layers of polysilicon and tantalum silicide.

Document D3 (see Figures 1(e) and 2(f)) describes a semiconductor device comprising a silicon substrate 1, an oxide film 2, 3, a polycrystalline silicon gate region 4, a PSG layer 6 and aluminium wiring 8. This document discusses the undesirable effects caused by the step of reflowing the PSG layer. With regard to Figures 1(c) and 1(d) (see also page 2, last line, page 3, lines 1 to 10 and 16 to 20), during reflow, an oxide film 7 is formed on exposed surface of the silicon substrate and, moreover, oxidation of the silicon layer 4 takes place (see, in particular, layer 71), which results in the gate region shrinking with

resultant increase of resistance. In order to avoid these problems, a silicon nitride film 9 is deposited before forming the PSG layer (see Figure 2(a) and 2(b)). Undesirable oxidation of the gate region under the PSG layer in reflow thermal treatment is thus suppressed.

Although it is known from D3 that the reflow process of the PSG layer can cause oxidation of the underlying polysilicon region, the document nevertheless teaches away from the invention as claimed, because it proposes a measure (i.e. the provision of the silicon nitride film) for **avoiding** such oxidation during reflow.

In the decision under appeal, the Examining Division essentially argues as follows:

(i) Should the skilled person, on using the method disclosed in D1, realise that thermal oxidation of the lower wiring layer occurs and that this oxidation causes a problem for the device, then the solution of using another oxidation method is immediately apparent (see page 9, third paragraph, page 11, third paragraph).

(ii) Control of the resistivity of the silicide layer can be achieved by selecting a silicide having a given composition which provides the required resistivity (see page 14, first paragraph). The fact that, at a later stage in the process, during reflow, the silicide layer is in fact oxidized is then a bonus effect which is achieved automatically (see page 11, last two lines, page 12, first paragraph, page 13, first paragraph).

(iii) The conditions (temperature, time, glass material) used in the steam heating reflow step according to D1 are so similar to those of reflow in the present application that they must be sufficient to cause oxidation of the lower wiring layer (see page 7, last paragraph, page 9, last paragraph, page 10, first paragraph).

These arguments are not convincing. It appears logical that the skilled person would consider replacing the thermal oxidation step known from D1, if he realizes that this step has an uncontrollable effect on the resistivity of the lower wiring layer. However, the cited prior art does not teach such a replacement. This means that, should the skilled person come to this idea, he would not know how to put it into practise. In this respect, the Examining Division admits that different solutions are possible, for instance using a silicide layer having a very well-defined composition. In any case, D1 does not suggest a lower wiring layer made of refractory metal silicide, nor omission of the thermal oxidation step of the lower wiring layer, nor a reflow step which also forms an oxide layer. The use of a tantalum silicide layer is known from D2, but even combining D1 with D2 would not lead to the claimed invention. Moreover, the fact that the reflow conditions in D1 are such that oxidation of the lower wiring layer might take place is not relevant, since according to D1 the thermal oxidation step is essential.

2.4 Therefore, the subject-matters of Claims 1, 6 and 8 according to the main request involve an inventive step (Article 56 EPC). The same conclusion applies for dependent Claims 2 to 5 and 7.

2.5 The main request is allowable and a patent can be granted on this basis.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the following documents according to the main request:

Claims:
No. 1 to 7, 8 (page 14) as filed with the letter of 20 October 1994,
No. 8 (page 15) as filed with the letter of 16 July 1998,

Description:
Pages 1 to 3, 5, 7, 8 as originally filed,
Page 4, 6, 9, 10 as filed with the letter of 16 July 1998,

Drawings:
Figures 1A, 1B, 1C, 1D, 1E, 1F as filed with the letter of 22 February 1990,
Figures 2A, 2B, 2C, 2D, 2E, 3A, 3B, 4A, 4B, 5A, 5B, 5C, 6A, 6B, 6C as originally filed.

The Registrar: The Chairman:

M. Beer G. Davies