BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS | BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE | CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [X] To Chairmen

D E C I S I O N
of 19 April 1996

Case Number: T 0898/94 - 3.5.2

Application Number: 86114529.0

Publication Number: 0219846

IPC: H03K 3/037

Language of the proceedings: EN

Title of invention:
Latch circuit tolerant of undefined control signals

Applicant:
MITSUBISHI DENKI KABUSHIKI KAISHA

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - yes"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0898/94 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 19 April 1996

Appellant: MITSUBISHI DENKI KABUSHIKI KAISHA
2-3, Marunouchi 2-chome
Chiyoda-ku
Tokyo (JP)

Representative: Lehn, Werner, Dipl.-Ing.
Hoffmann, Eitle & Partner
Patentanwälte
Postfach 81 04 20
D-81904 München (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 1 March 1994 refusing European patent application No. 86 114 529.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: R. G. O'Connell
B. J. Schachenmann

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division refusing European patent application No. 86 114 529.0. The reason given for the refusal was that the subject-matter of the claims then on file did not involve an inventive step, having regard to the following prior art:

B2: Patents Abstracts of Japan, vol. 6, No. 145 (P-132) [1023], 4 August 1982; abstract of JP-A-57 64394

B2a: JP-A-57 64 394, full document and translation into English.

The following document was also referred to during the examination proceedings:

B1: WO-A-8 403 012.

II. Claim 1 (main request) is worded as follows:

"1. A latch circuit including:

a master latch circuit (M) including a first reading gate (G_1) for receiving an input signal (A) and for providing an output signal (O_1) to a first connection point and a first latching gate (G_2) for receiving an input derived from said first connection point and for providing an output (O_2) to said first connection point;

first means for controlling said master latch circuit (M) by a control signal (ϕ) alternately to enable said first reading gate (G_1) and disable said first latching

gate (G_2) and to disable said first reading gate (G_1) and enable said first latching gate (G_2) to thereby enable a first latching output (O_2) at said first connection point;

a slave latch circuit (S) including a second reading gate (G_3) for receiving an input from said first connection point and for providing an output signal (O_3) to a second connection point and a second latching gate (G_4) for receiving an input derived from said second connection point and for providing an output signal (O_4) to said second connection point;

second means for controlling said slave latch circuit (S) by said control signal (ϕ) alternately to enable said second latching gate (G_4) and disable said second reading gate (G_3) and to disable said second latching gate (G_4) and enable said second reading gate (G_3) to thereby enable a second latched output (O_4) at said second connection point;

characterized in that the output impedances (Z_1 to Z_4) of said gates (G_1 to G_4) satisfy the following condition when the magnitude of the voltage of said control signal (ϕ) lies within a predetermined range, $\phi_1 < \phi < \phi_2$, of which the lower end value (ϕ_1) is the control signal voltage at which the output impedances (Z_3, Z_4) of the second reading and latching gates (G_3, G_4) transiently become equal and the upper end value (ϕ_2) is the control signal voltage at which the output impedances (Z_1, Z_2) of the first reading and latching gates (G_1, G_2) transiently become equal, said condition being:

$$Z_1 > Z_2 \quad \text{and} \quad Z_3 > Z_4,$$

whereby for any voltage value of said control signal (ϕ), said first reading gate (G_1) provides an output

signal (O_1) to said first connection point at times other than when said second reading gate (G_3) provides said output signal (O_3) to said second connection point."

Claims 2 to 4 are dependent on claim 1.

III. The appellant argued essentially as follows:

A conventional master-slave latch circuit of the kind shown in Figure 12 of the present application and as specified in the preamble of claim 1 of the main request suffered from the disadvantage that an input signal applied to the master latch circuit might be transferred directly to the slave latch circuit resulting in no latching operation. It was considered that this fault resulted from the reading gate transistors being larger than the latching gate transistors for propagation speed reasons. The present invention solved this problem by setting the impedances of the reading gates to be larger than the impedances of the latching gates during the central portion of the clock transition interval, this dimensioning rule being specified in the characterising part of claim 1.

The prior art B2a relied on by the examining division addressed a different problem of erroneous latch operation due to some signal transmission delay (Figure 7, equivalent delay circuits 20 and 21). The latter might cause the data held in the master subcircuit to be erroneously altered and in order to prevent this a resistor was additionally provided in the vicinity of the reading gate transistor to ensure that a potential level at a particular junction D exceeded a threshold level of an inverter to prevent the data corruption.

The view of the examining division that the impedance relationship in the prior art document met the claim 1 specification was not tenable since none of the prior art references - not even B2a - disclosed the relationship between the impedances during the clock transition interval.

The decision under appeal based its reasoning on the unjustified assumption that the transistors 2 and 7 shown in document B2a were electrically identical. The mere fact that two transistors were depicted in the same way did not lead the skilled person to infer that their impedances should be the same. It followed that increasing the resistance of the reading gates did not necessarily lead to the inequalities specified in claim 1 being met.

Thus B2a addressed a different problem and taught a different solution.

IV. The appellant requested that the decision under appeal be set aside and a patent granted on the basis of the application as refused (main request), consisting of the following documents:

Claims: claim 1 (part I) and claims 2 to 4 filed 12 October 1993,
claim 1 (part II) submitted at first instance oral proceedings 9 November 1993;

Description: pages 1 to 3 and 5 to 10 as originally filed, page 4 submitted at first instance oral proceedings 9 November 1993, page 4a filed 10 November 1993, page 4b filed 6 September 1991;

Drawings: Sheets 1 to 7 filed 11 November 1986.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments (main request)*

The application according to the main request does not contain subject-matter which extends beyond the content of the application as filed. In particular, the first paragraph of the characterising portion of claim 1, which did not appear in the originally filed claims, is directly and unambiguously derivable from the passage at page 7, line 4, to page 8, line 16 of the description as originally filed. In the judgement of the board, the present form of the application does not contravene Article 123(2) EPC.

3. *Novelty (main request)*

None of the cited prior art documents discloses a latch circuit comprising all the features recited in claim 1; see also point 4.8 below. Hence the subject-matter of the claim is new within the meaning of Article 54 EPC.

4. *Inventive step (main request)*

4.1 A latch circuit comprising all the features of the prior art portion of claim 1 is undisputedly known from B1, Figure 1a and from B2a, the most relevant embodiment of the latter being that described at page 17 as a variant of the circuit shown in Figure 8 of the drawings. Starting from a latch circuit as specified in the preamble of the claim, the problem addressed by the present application is to overcome the drawback of such a circuit that, under certain circuit conditions, the input signal read into the master subcircuit can be

transmitted directly to the slave subcircuit output, thus defeating the purpose of master-slave operation, which is to provide a slave output corresponding to the previous, not the current, master input; see page 4, lines 1 to 4, of the application as originally filed. According to the teaching of the present application this problem is solved by dimensioning the (control voltage dependent) output impedances of the respective reading and latching gates in the master and slave subcircuits, so as to satisfy the inequalities specified in claim 1 during a specified interval of the control voltage transition.

4.2 It is not disputed by the appellant that it pertains to the common general knowledge in the art of master-slave latch circuitry that such a race-through condition or undesired transparency between input and output is something to be guarded against; it is mentioned, for instance, in B1, paragraph bridging pages 9 and 10, although not in B2a (see point 4.5 below). Hence no contribution to inventive step is involved in formulating the problem identified above.

4.3 The solution taught by B1 involves using a highly asymmetrical clock waveform (Figure 5b) and there is undisputedly no suggestion in B1 which would lead the skilled person in the direction of the presently claimed solution.

4.4 The issue to be decided in this appeal, therefore, is whether, despite the fact that B2a does not explicitly address the problem identified above, the skilled person would nevertheless be led to devise a circuit falling within the terms of claim 1 by an obvious application of the teaching of B2a. The examining division envisaged this happening in two possible ways, either by

similarity in the problems addressed or by overlap in the circuit dimensioning solutions to the two different problems.

4.5 The board notes, however, that although the preamble of claim 1 can be read onto all the latch circuits described in B2a, every one of these circuits has at least one inverter stage between the master (M1) subcircuit read-in gate and the slave (M2) subcircuit read-in gate and the problem analysis in B2a is intimately connected with the effect of these inverters in the circuit. B2a does not address the problem of transparency or race-through in the sense of the present application. It refers, in the paragraph bridging pages 4 and 5, to possible overlap of the ON states of read-in and latch transistors - which is one of the contributory causes of transparency - but its teaching differs in several significant respects from that of the present application:

(i) It attributes the overlap to a different cause, namely, differential delay between clock signals at different points of the circuit; see B2a page 6, lines 15 to 24 and page 7, lines 5 to 16.

(ii) It is concerned with remedying a different effect of this overlap, namely the "H" level of the master subcircuit being corrupted by an "L" level in the slave subcircuit ("first erroneous operation" - B2a, page 7, line 17 to page 9, line 19) and latchup of an internal node E to a level below "H" level when master and slave subcircuit are both at "H" level("second erroneous operation" - B2a, page 9, line 20 to page 11, line 2). These "erroneous operations", as explained in detail in B2a, depend on up to four different clock signals Φ, Φ', Φ bar and Φ bar' being operative

simultaneously at different parts of the circuit and depend on potential changes induced by the operation of the inverters.

4.6 B2a, at page 17, teaches a solution for these problems of "erroneous operation" which is to dimension the conductances of the transistors of the read-in gates of master and slave subcircuits so as to provide the effect of an external series input resistor at each gate which counteracts the potential changes referred to immediately above.

4.7 In the judgement of the board, it would involve an unfair measure of hindsight to abstract the preamble latch circuit out of the B2a inverter-output latch circuit context, and to equate the actual problem of B2a with a different transparency problem in the abstracted circuit, given the importance of the inverters in the failure mode analysed in the prior art document. For this reason, the board is not persuaded that the skilled person would regard the teaching of B2a as relevant to the problem addressed by the present application. Such an attack on inventive step involves an ex post facto generalisation followed by an equally ex post facto specialisation to a new problem and is accordingly not convincing.

In coming to this conclusion the board is mindful of the fact that the present application includes embodiments such as Figure 5 in which the connection path from the output of the master reading gate to the input of the slave reading gate is not direct, but via a buffer circuit. The scope of claim 1 in this respect does not detract from the argument above that the problem addressed by B2a arises in part within the intermediate inverter stages, whereas the Figure 5 embodiment merely

shows that intermediate inverter/buffer stages are optional in giving effect to the teaching of the present application.

4.8 There remains the question of solution overlap. Would the skilled person arrive at a circuit encompassed by the dimensioning rule in claim 1 as an obvious application of the teaching of B2a, but for reasons unconnected with the problem ostensibly addressed by the description of the present patent application? In the present case the examining division found that the subject matter of the claim was new - a finding which the board upholds, since the dimensioning rule of claim 1 is not directly and unambiguously derivable from the cited prior art, nor is any specific circuit disclosed in the prior art which unambiguously meets this rule.

4.9 The examining division nevertheless found that, on the assumption that the transistors 2 and 7 of B2a were electrically identical, there being no reason to believe otherwise, the variant of the circuit disclosed in B2a, Figure 8, described at page 17 without a drawing, would appear to the skilled person to be so designed as to reproduce the behaviour tabulated in Figure 2 of the present application and hence meet the terms of the dimensioning rule in claim 1 as well as the functional statement in the last five lines of the claim; points 12 to 14 of the decision under appeal.

4.10 In the judgement of the board this conclusion is not safe. The table of Figure 2 of the present application is not comprised in the state of the art. Neither, for that matter, is the table of Figure 13, which, although labelled "prior art" is an analysis of the failure mode of a circuit (Figure 12) corresponding to the preamble of claim 1. The latter circuit does not figure in this

precise form i.e. with a direct connection between the output of the master read-in gate and the input of the slave read-in gate in the cited prior art (see points 4.5 and 4.6 above). As has been pointed out in decision T 654/92 (unpublished), point 4.3, inventive step assessment should be based on the prior art which has been established as having been made available to the public, not on internal prior art. This principle applies with even more force in relation to an analysis of failure modes of internal prior art which appears only in the description of the application, such analyses frequently representing insights, eg identifying a sub-problem which makes a contribution to inventive step. In the present case there is no evidence that the analysis underlying the table of Figure 13 had been made available to the public. To maintain, therefore, that the circuit disclosed in B2a, Figure 8 " would appear to the skilled person to be so designed as to reproduce the behaviour tabulated in Figure 2 of the present application" is, in the judgement of the board, a speculation prompted by hindsight. If the tabulated behaviour were reproduced it would be by accident not by design.

4.11 In applying the problem and solution approach to assessment of inventive step it is frequently necessary and appropriate to modify the subjective problem initially addressed in the patent application as originally filed in favour of the objective problem implied by the claim in the light of the subsequently determined prior art. This problem-shifting as a basis for an attack on inventive step should, however, stay within the bounds of what the skilled person would realistically contemplate. If, as in the present case, a prior art document narrowly fails to destroy novelty by accidental anticipation, it is perfectly legitimate to consider whether an obvious variant of what is

specifically disclosed would be encompassed by the claim. However, when assessing what variants the skilled person would realistically contemplate it is essential to remain within those considerations and systematic variations which would be relevant to the problem derived from that document. In the judgement of the board, the decision under appeal crossed this boundary when it attempted to analyse the transient behaviour of the relative output impedances of the transistors 2 and 7 in Figure 8 of B2a, thereby relying on questionable **ad hoc** assumptions as to their initial and final values. The latter document is silent about the relative output impedances of these transistors, either before or after the modification of the conductance value of the transistor 2. The present application indicates at page 3 that the impedance of the reading gate transistor (corresponding to 2) is likely to be lower than that of the latch gate transistor (corresponding to 7) for propagation delay reasons, in which case increasing the resistance of the transistor 2 would not necessarily result in the output impedance of the latter being greater than that of the transistor 7 during the central part of the clock transition, as required by claim 1. If, on the other hand, it is legitimate to assume, as the examining division did, that the transistors 2 and 7 have identical parameters, it is equally arguable that the skilled person would choose to retain this identity, eg for ease of fabrication, while modifying the absolute conductance values in accordance with the teaching of B2a. Since the latter document does not concern itself with these relative impedances it remains a matter of speculation. In effect, the examining division demonstrated that the skilled person, in applying the teaching of B2a, in particular in dimensioning the conductances of transistors 2 to produce the effect of increased static input resistance, **could** arrive at a circuit encompassed by claim 1, whereas the onus is to

show that by systematic application of the prior art teaching he **would** arrive at such a circuit. Putting it another way, the disclosure in B2a of a generic class or set of circuits which solve the problem addressed in that document is not a bar to the subsequent patenting of a different generic class or set of circuits which solve a different problem, even if the classes overlap, provided that no circuit of the intersection set is either specifically disclosed in B2a (accidental anticipation) or is specifically and systematically derivable in an obvious manner from the teaching of B2a by a person skilled in the art addressing the problem of B2a.

4.12 The board concludes therefore that, having regard to the cited prior art, the subject-matter of claim 1 is not obvious to a person skilled in the art and is thus considered as involving an inventive step within the meaning of Article 56 EPC.

5. In the judgement of the board, the application documents of the main request in their present form meet the requirements of the EPC. The main request being allowable, the auxiliary requests need not be considered.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in accordance with the appellant's main request (see paragraph IV above).

The Registrar: The Chairman:

M. Kiehl W. J. L. Wheeler