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D E C I S I O N
of 10 July 1996

Case Number: T 0946/94 - 3.5.2

Application Number: 89480044.0

Publication Number: 0387461

IPC: H03K 19/013

Language of the proceedings: EN

Title of invention:
Improved BICMOS logic circuit with full swing operation

Applicant:
International Business Machines Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56, 109(1), 111(1)

Keyword:
"Inventive step - yes, over prior art relied on in the decision under appeal"
"Interlocutory revision - would have been appropriate"
"Remittal to department of first instance to complete the examination"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0946/94 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 10 July 1996

Appellant: International Business Machines Corporation
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Armonk, N.Y. 10504 (US)

Representative: Klein, Daniel Jacques Henri
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Département de Propriété Intellectuelle
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 3 May 1994 refusing European patent application No. 89 480 044.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: R. G. O'Connell
B. J. Schachenmann

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division refusing European patent application No. 89 480 044.0. The reason given for the refusal was that the subject-matter of the independent claim then on file did not involve an inventive step, having regard to the following prior art:

D5: EP-A-0 058 958,
D6: EP-A-0 212 584.

II. With the statement of grounds the appellant filed amended claims 1 to 4.

III. Claim 1 is now worded as follows:

"An improved BICMOS logic circuit (D1, ...) having full swing operation of the kind including:

a conventional BICMOS logic circuit (11, ...) biased between first and second supply voltages (VH, GND) comprising a logic gate block (13) driven by a plurality of logic input signals (A1, A2, ...), and a driving block (12) connected in series with the said logic gate block comprised of two bipolar transistors (T1, T2) referred to as the top and bottom output transistors connected in series with an output node (14) connected therebetween; an output terminal (15) connected to said output node where the circuit output signal (S) is available; the said conventional BICMOS logic circuit operating normally in a partial swing mode,

characterised in that it further includes:

a CMOS logic interface circuit (C2, C2') comprised of two cross coupled inverters (INV1, INV2) forming a latch, the feed back loop of which is connected to said output node (14) connected to said output terminal to force the said output signal (S) to full swing between said first and second supply voltages to give to the said improved BICMOS logic circuit the desired CMOS compatibility."

Claims 2 to 4 are dependent on claim 1.

IV. The appellant argued essentially as follows:

The closest prior art D5 dealt only with half BICMOS circuits, whereas the claims were now limited to full BICMOS in which the output stage comprised two bipolar transistors. More significantly, the solution taught in D5 to the problem of increasing voltage swing at the output was to provide FET logic circuitry connected to the output terminal which duplicated the input circuitry of the driving logic. This solution corresponded to the embodiment of figure 5 of the present application as originally filed, which was not encompassed by the present claims. The D5 approach suffered from the disadvantages that the duplicate circuitry had to increase in complexity with the complexity of the driving logic function and that the duplicate circuitry loaded the input node, slowing down the circuit operation. The circuit now claimed in claim 1 overcame these disadvantages by providing the desired full swing by means of a latch whose structure was independent of the input logic circuit and which did not load the input circuit. The use of such a latch was neither shown nor suggested in D5.

The argument in the decision under appeal that, starting from D5, the person skilled in the art would be led by the teaching of D6 to replace the output interface circuit of D5 by a latch as specified in the characterising part of claim 1 was based on a misinterpretation of D6 combined with an inadmissible ex post facto analysis. D6 was not concerned with the problem of full swing for the very good reason that the D6 circuit, being comprised of two serially connected FETs 5 and 7 (Fig 3) - ie, not a BICMOS circuit - was naturally full swing. D6 was concerned rather with stabilising the output potential by suppressing undershoot/overshoot. Although the means employed in D6 to effect this stabilisation comprised two inverters 15, 3 (Fig 6) the latter did not have a latch function, as could be understood from the description of these figures in D6 and as was confirmed by the fact that the waveforms of Fig 4 and Fig 6 were identical. Neither the term "full swing" nor "latch" occurred in D6, nor was there any suggestion in D6 that a latching function was desirable or relevant. The examining division's misinterpretation of D6 clearly relied on the disclosure of the present application.

V. The appellant requested that the decision under appeal be set aside.

Reasons for the Decision

1. The appeal is admissible.

2. *Inventive step*

2.1 In essence the board approves and adopts the reasoning of the appellant on the issue of inventive step as set out in the statement of grounds of appeal and as summarised at point IV above, which it finds cogent.

2.2 In the judgement of the board D6 is not a relevant document. It neither relates to BICMOS circuits nor to the problem of reduced voltage swing which arises in such circuits. The problem which D6 addresses, viz undershoot and overshoot of output signal levels caused by parasitic wiring inductance in pure CMOS logic, cf D6, pages 1 to 3, is not reasonably comparable with the problem of reduced voltage swing caused by V_{BE} drops in the double bipolar output stage of a BICMOS circuit. The contention in the decision under appeal at point 10 that the problem associated with conventional BICMOS circuits has to be understood as a **permanent undershoot** in the output signal levels is, at best, an analogy based on hindsight. Even with knowledge of the disclosure of the present application it remains a somewhat artificial verbal construction which conflates two fundamentally different technical effects. Undershoot and overshoot are essentially dynamic phenomena, relating to **settling time** of a signal, whereas signal swing is an essentially static consideration, relating to amplitude limits irrespective of timing considerations.

2.3 Moreover, the solution taught by D6 to this different problem is itself only superficially analogous to that specified in claim 1, since, as pointed out by the appellant, the prior art solution does not rely on a latch function provided by the pair of inverters forming the output interface circuit in D6 (cf Figs 5 and 6 and associated description).

2.4 It does not appear plausible to the board that the person skilled in the art, starting from D5, with its inadequate solution to the problem of reduced swing, would derive the claimed circuit solution from consideration of a document such as D6 which teaches a different solution to a different problem.

2.5 The board concludes therefore that, at least having regard to the prior art documents D5 and D6, the circuit of claim 1 is not obvious to a person skilled in the art.

3.1 In view of the cogent argumentation in the very concise statement of grounds of appeal (less than three full pages) the examining division would have done well to set its decision aside pursuant to Article 109(1) EPC and resume the examination procedure. In these circumstances the board deems it inappropriate to exercise its powers under Article 111(1) EPC to complete the examination of the application and will instead remit the case for this to be done by the examining division.

3.2 Since the examining division acted within its discretion under Article 109(1) EPC in deciding not to set its decision aside, no procedural violation was involved and accordingly the question of reimbursement of the appeal fee does not arise; indeed the appellant has made no request for such a reimbursement.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution.

The Registrar: The Chairman:

M. Kiehl W. J. L. Wheeler