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D E C I S I O N
of 24 February 1999

Case Number: T 0030/95 - 3.4.1

Application Number: 89830330.0

Publication Number: 0362147

IPC: H01L 21/82

Language of the proceedings: EN

Title of invention:
Fabrication of CMOS integrated devices with reduced gate length

Applicant:
STMicroelectronics S.r.l.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54(1), 111(1)

Keyword:
"Novelty (yes - after amendments)"
"Remittal of the case"

Decisions cited:
-

Catchword:
-

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Case Number: T 0030/95 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 24 February 1999

Appellant: STMicroelectronics S.r.l.
Via C. Olivetti, 2
20041 Agrate Brianza (Milano) (IT)

Representative: Pellegri, Alberto
c/o Società Italiana Brevetti S.p.A.
Via Puccini, 7
21100 Varese (IT)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 6 September 1994 refusing European patent application No. 89 830 330.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. Davies
Members: U. G. O. Himmler
M. Rognoni

Summary of Facts and Submissions

I. European application No. 89 830 330.0 (publication No. 0 362 147) was refused by a decision of the Examining Division dated 6 September 1994.

The decision was based on the application documents including claims 1 and 2 as originally filed.

II. The reason given for the refusal was that claim 1 was not allowable since its subject-matter was not novel in the sense of Article 54(1) and (2) EPC with respect to the disclosure of document D2, i.e. D2: US-A-4 598 460.

The Examining Division's arguments may be summarised as follows:

The subject-matter of claim 1 was fully anticipated by document D2, in particular by the Figures 1 to 15 and the corresponding description. Document D2 disclosed a process for fabricating polycristalline silicon and /or silicide gate CMOS integrated devices on a doped monocrystalline silicon substrate of a first p-type polarity wherein deep well diffusions of a second n-type polarity are formed in which transistors having a channel of said first p-type polarity are formed and outside of which transistors having a channel of said second n-type polarity are formed, comprising the steps of performing an unmasked ion implantation of a dopant of said first p-type polarity (boron) over the entire surface of said silicon substrate after having formed said deep well diffusions in order to produce simultaneously a partial compensation of the superficial doping level of said well regions and an enrichment of the superficial doping level of said substrate outside of said well regions.

The applicant's argument, i.e. that in the process according to document D2 the unmasked implantation is performed immediately before the gate oxidation whereas in the process of the invention this implantation is performed immediately after having formed the well diffusion and before growing the field oxide, was not considered to be relevant since it related to features which were not in the claim. The independent claim 1 did not comprise any feature which would lead to devices distinguishable from devices obtained by the process known from document D2.

III. On 4 November 1994 the appellant filed a notice of appeal against that decision, the appeal fee having been received by the EPO on 28 October 1994. A statement of grounds of appeal was filed on 28 December 1994.

IV. The Appellant filed new claims 1 and 2 with the grounds of appeal.

The appellant's arguments in support of patentability of the subject-matter of the newly-filed claims may be summarised as follows:

Contrary to the process described in document D2 which describes the realization of a "buried" p-channel transistor in prediffused n-well regions having a doping level exactly predetermined in order to produce the desired threshold voltage of the p-channel transistor formed therein, the present invention discloses a fabrication process that is based on carrying out a threshold adjustment implantation, **simultaneously**, in the channel regions of both the p-channel transistors to be formed into preformed n-well regions and the n-channel transistors to be formed outside said preformed n-well regions. This is effected by a single boron implantation step that only **partially**

compensates the n-type doping of the preformed n-well region in a superficial layer thereof that will thus constitute a **superficial** channel region of the p-channel transistors. The same boron implantation enriches a similar superficial portion of the p-type substrate, to a level that will produce a correct threshold of superficial n-channel transistors as well. Therefore, the resulting CMOS structures have n-channel and p-channel structures that as far as certain electrical parameters are concerned, e.g. breakdown voltage, are substantially similar. Further, the transistors' size is strongly reduced by the novel process of the invention in comparison to the "buried" channel structures.

The superficial channel transistors of the present invention have certain advantages over those structures produced according to the state of the art, e.g. the attendant leakage due to the persistence of a current path between drain and source regions is excluded.

V. In a communication pursuant to Article 110(2) EPC, the appellant was informed of the Board's provisional view that claim 1 required an amendment for clarity, and that such an amended claim would meet the requirement of novelty within the meaning of Article 54(1) EPC. The appellant was also informed that the Board would carry out further examination of the application pursuant to Article 111 EPC, unless the appellant requested that the case be remitted to the department of the first instance.

VI. In response to this communication, the appellant filed, with a letter dated 17 November 1997, a new claim 1, amended as proposed by the Board, to replace claim 1 previously on file.

The appellant requests that the decision under appeal be set aside, and that the case be remitted to the Examining Division for further prosecution.

VII. New claim 1 filed with the letter dated 17 November 1997 reads as follows:

"1. A process for fabricating polycrystalline silicon and/or silicide gas CMOS integrated devices having a threshold that is predefinable by the processing, on a doped monocrystalline silicon substrate of a first type of conductivity, wherein deep well diffusions of a second type of conductivity are formed, in which transistors with a channel of said first type of conductivity are formed and outside which transistors having a channel of said second type of conductivity are formed,
characterized by realizing also the transistors of said first type of conductivity with a superficial channel while permitting threshold definition of transistors of both types of conductivity, by performing an unmasked ion implantation of a dopant of said first polarity over the entire surface of the silicon substrate after having formed said deep well diffusions with a dose and under implant conditions capable of simultaneously producing a partial compensation of the superficial doping level of said well regions to produce a superficial channel of said first type of conductivity providing for a certain threshold and an enrichment of the superficial doping level of said substrate outside said well regions to produce a superficial channel of said second type of conductivity in areas where said transistors will be formed providing for a certain threshold."

Reasons for the Decision

1. The appeal complies with the requirements of Articles 106 to 108 and Rule 64 EPC and, therefore, is admissible.

2.1 The valid claim 1 is essentially distinguished from claim 1 as refused by the Examining Division by features which refer to effects to be attained by the product of the claimed process. These effects have the following features:

- that the produced CMOS integrated devices have a threshold voltage that is predefinable by the processing;

- that the ion implantation dose of the dopant and the implant conditions are chosen in such a way as to produce transistors with a superficial channel of first or second conductivity type providing for a certain threshold voltage.

2.2 Document D2 discloses a blanket ion implantation with a P-conductivity type impurity (e.g. boron) using field oxide as ion implantation mask in order to adjust the doping level of the P-conductivity type impurity in the channel region of the EPROM, and thereby adjust its threshold independently of the threshold of the P-channel device and the N-channel device; cf. column 4, lines 9 to 35 with reference to Figure 6. According to Figure 6, the channel region 36 of the p-channel transistor in the N-well 18 receives P-conductivity type implant during this blanket ion implantation.

It follows from the text in column 4, lines 26 to 31, of document D2,

"However, as previously described with respect to Figure 1, this region 36 was doped independently in an earlier step, at which time the doping of N-well 18 was performed. During that independent doping of region 18, the implant shown in Fig. 6 was considered and **compensated for"** (emphasis added by the Board),

that the dose of the phosphorus ion implantation described with reference to Figure 1 (see column 3, lines 6 to 27) is determined by taking into consideration the subsequent dose of boron ion implantation described with reference to Figure 6. Thus the boron ion implantation **partially** compensates for the earlier N-type implantation.

2.3 On the other hand, it follows from the description in document D2 that the process as now claimed in claim 1 is distinguished from this state of the art in that the ion implantation of a dopant of first polarity is carried out without a mask, which implies that the **entire surface of silicon substrate receives ion implantation**. In document D2, on the other hand, the blanket boron ion implantation is performed using a field oxide 14 as a mask.

In the Board's view, therefore, the subject-matter of claim 1 is new in respect to document D2 within the meaning of Article 54(1) EPC.

3. The decision of the Examining Division to refuse the application had been based on an independent claim 1 which did not yet comprise a number of features comprised by the presently valid claim 1. In particular, the refused claim was not restricted to a process:

- realizing transistors of first conductivity type with a superficial channel while permitting a threshold definition of transistors of both conductivity types,

- producing a superficial channel of the second conductivity type in areas where the transistors will be formed and providing for a certain threshold.

Even if these additional features are essentially functional features, the claimed subject-matter is restricted by these features and, therefore, the request of the applicant that the matter should be remitted to the department of the first instance so as to preserve its right to a two-instance examination is justified. A further reason for remittal of the case is that so far no conclusive examination in respect of the other requirements of the Convention has been carried out.

4. For this reason, the Board deems it appropriate to make use of the power conferred upon it by Article 111(1) EPC to remit the case to the first instance for further examination in respect of the further requirements of the Convention.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the Examining Division for further prosecution on the basis of claims 1 and 2 filed with the appellant's letter dated 17 November 1997.

The Registrar: The Chairman:

M. Beer G. Davies