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D E C I S I O N
of 18 December 2000

Case Number: T 0053/95 - 3.4.3

Application Number: 90830177.3

Publication Number: 0401174

IPC: H01L 29/784

Language of the proceedings: EN

Title of invention:

Surface field effect transistor with depressed source and/or drain areas for ulsi integrated devices

Applicant:

STMicroelectronics S.r.l.

Opponent:

-

Headword:

Double diffused drain/STMICROELECTRONICS

Relevant legal provisions:

EPC Art. 56

Keyword:

"Inventive step (no)"

Decisions cited:

-

Catchword:

-



Case Number: T 0053/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 18 December 2000

Appellant: STMicroelectronics S.r.l
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 22 September 1994
refusing European patent application
No. 90 830 177.3 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
A. C. G. Lindqvist

Summary of Facts and Submissions

I. European patent application No. 90 830 177.3 was refused by a decision of the examining division dated 22 September 1994. The ground for the refusal was that the subject matter of claims 1 to 7 lacked an inventive step with respect to the prior art documents

D1: Patent Abstracts of Japan, vol. 8, no. 8 (E-221) [1445] 13 January 1984 & JP-A-58-171 863; and

D2: IEEE Circuits and Device Magazine, vol. 1, no. 6, November 1985, pages 13 to 16.

II. The appellant (applicant) lodged an appeal on 15 November 1994 paying the appeal fee on 14 November 1994. A statement of the grounds of appeal was filed on 10 January 1995.

The appellant requested that the decision under appeal be set aside and a patent be granted based on the following documents:

Claims: 1 to 5 (first part) filed on 8 April 1994 with the letter dated 1 April 1994
5 (second part) to 8 filed on 30 September 1993 with the letter dated 29 September 1993

Description: pages 1, 2, and 4 as originally filed
pages 3, 3 bis, 5 to 10 filed on 30 September 1993 with the letter dated 29 September 1993

Drawings: Sheets 1/4 to 4/4 filed on 30 September 1993 with the letter dated 29 September 1993.

III. In a communication dated 18 February 2000, the Board introduced an English translation of document D1 (in the following referred to as document D1a) into the appeal proceedings and informed the appellant of its provisional opinion that the subject matter of claim 1 did not seem to involve an inventive step. In response, the appellant filed further observations with the letter dated 6 June 2000.

IV. Claim 1 of the appellant's request reads as follows:

"1. An integrated circuit transistor structure, comprising
a body of semiconductor material;
double diffused source and drain regions (4,7) of a first conductivity type at a first surface of said body, said source and drain diffused regions (4,7) defining a channel region (5) of opposite conductivity type therebetween;

a gate structure (1,2) overlying said first surface above said channel region, and capacitively coupled to said channel regions, said gate structure comprising a dielectric sidewall spacer (6) on the sidewall of said gate structure (1,2) adjacent to said drain and source regions;

wherein said first surface of said body is recessed over at least said drain region, to a depth of between 50 and 500 nanometers below the level of said first surface under said gate structure (1,2) and wherein said spacer (6) extends down below the rest of said gate structure (1,2) to said recessed surface over said double diffused drain region."

Claims 2 to 8 are dependent claims.

V. The appellant presented essentially the following arguments in support of his request:

- (a) The application in suit is primarily concerned with the problems (c) to (e) referred to in the application, all relating to the occurrence of high electric fields around the drain region and "hot electrons", i.e. the "snapback" phenomena (problem (c)), stability of threshold voltage (problem (d)), and preservation of the integrity of the gate oxide layer even after injection of "hot electrons" (problem (e)). Document D1, on the other hand is primarily concerned with increasing the drain withstand voltage which is unrelated to the reduction of hot electrons. The mere fact that the solutions to the problems due to hot electrons may also produce a positive effect on high voltage withstanding capabilities does not make the technical problems addressed in document D1 the same as that of the present application. Thus, a skilled person starting from the device of document D2 and faced with the above problems (c) to (e) would not consider document D1 to be relevant to the problems.
- (b) Even assuming that a skilled person would find a motivation to combine the teaching of document D2 with that of document D1, the resulting device would fail to have all the features of the claimed device, since he would proceed to etch the silicon substrate after the first phosphorous diffusion and before effecting the second implant. Therefore, contrary to the device of claim 1, the sidewall spacers would not extend into the recesses.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.
2. *Inventive step*

The only issue in the present appeal is that of inventive step.

- 2.1 The application in suit relates to MOSFETs suitable for ULSI (ultra large scale integration) which have a channel length of 1 μm or less. Due to the short distance between source and drain regions, such small MOS-device are known to have problems commonly known as "short-channel effects", such as (a) low gain; and (b) low punch through voltage, and problems caused by high electric fields in a region adjacent the drain region and the gate oxide layer (cf. the application as published, column 1, lines 15 to 43). The application in suit focuses on the latter problems caused by the high electric field, i.e. (c) avalanche multiplication (also called "snap back") thereby destroying the device (cf. column 1, lines 29 to 31); (d) generation of energetic electrons (so-called "hot electrons") which enter the gate oxide layer and thereby change the device characteristics such as threshold voltage and gain (column 1, lines 32 to 43); and (e) impairment of the integrity of the gate oxide layer after injection of hot electrons (column 1, lines 36 to 43; column 3, lines 4 to 11).

To solve in particular the above problems (c) to (e), the application in suit proposes (I) formation of recessed source and drain regions with respect to the

channel; and (II) use of a graduated drain structure, also called double diffused drain (DD), i.e. the inner part of the drain is surrounded by a lower doped region forming a graded pn-junction.

2.2 Document D2 represents the closest prior art and this has not been disputed by the appellant. It discloses a double-diffused drain MOSFET with a planar upper surface where spacers are provided on the sidewalls of the gate electrode (cf. D2, figure 1(a)). The double-diffused drain structure has the purpose of improving the source/drain breakdown voltage and reducing the hot electron-induced degradation for devices having a length scale of a micrometer and below (cf. D2, page 13), i.e. document D2 addresses the same problems (c), (d) and (e) as the application in suit.

2.2.1 The device of claim 1 differs from that of document D2 in that

(A) at least the drain region is recessed 50 to 500 nm below the surface of the channel whereas document D2 shows a planar device; and

(B) the spacer (sidewall on the gate) extends down below the gate to the recessed surface.

2.3 Since the prior art document D1 (JP-A-58-171 863) is written in the Japanese language, all the cited passages below are taken from document D1a which is an English translation of document D1.

2.3.1 Document D1 discloses a MOSFET having recessed source and drain regions 2, 3 with respect to the channel region (cf. Figure 4). The recess is about 400 nm deep which is within the range specified in claim 1 of the present application (cf. D1a, page 6, lines 5 to 8). The recessed source and drain structure has the effect

of increasing the withstand voltage of the drain region (also known as punch-through voltage) (cf. D1a: page 2, lines 32 to 35; page 4, line 33 to page 5, line 1). It is moreover pointed out in document D1 that, for a conventional, planar MOSFET, the drain withstand voltage is limited by electric field concentration at the portion of the drain region adjacent to the gate oxide layer (cf. page 4, lines 9 to 13 and Figure 2). The device of document D1, on the other hand, has the feature that the drain region is separated from the gate oxide layer which limits the electric field concentration in this region (cf. D1a, page 5, lines 15 to 20).

From the above, it follows that document D1 is concerned with lowering the electric field adjacent the end portion of the drain region adjoining the channel region, i.e., the same problem as addressed in document D2 (cf. D2, page 13, first sentence). Moreover, the above technical problem is addressed in document D1 with the aim to maintain the small size of the device for high scale integration (cf. D1a, page 2, lines 32 to page 3, line 6).

In contrast to the device according to claim 1, however, document D1 does not disclose any double diffused source/drain structure.

2.3.2 It follows from the above that contrary to the appellant's argument, document D1 relates not only to the problem of improving the punch-through voltage, but also to the problems addressed in both document D2 and the application in suit (cf. item V(a) above).

2.4 In view of the discussion under points 2.1 and 2.2.1 above, the objective technical problem addressed by the invention in suit in relation to the closest prior art document D2, relates to reducing further the electric

field near the channel-gate oxide interface, thereby effecting a reduction of hot electrons injected into the gate oxide layer, as well as obtaining such a reduction of the electric field without loss of wafer surface (cf. application in suit, column 3, line 51 to column 4, line 11).

- 2.5 A skilled person faced with the task of improving the above-mentioned properties of the device of document D2, Figure 1, would in the Board's opinion consider the teaching of document D1 to be relevant, since both documents are concerned with lowering the electric field in the channel region which are known to reduce the hot electron effects. Therefore, the skilled person would appreciate that double diffused source/drain regions in a recessed source/drain structure would lead to a further improvement with respect to the device of document D2 regarding the reduction of hot electron effects, as well as leading to an improvement of the breakdown voltage characteristics.

When applying the teaching of document D1 on the double diffused MOSFET device of document D2, the skilled person would necessarily etch the recesses for the source/drain regions before the first phosphorous diffusion is carried out, i.e. the step of etching the recesses is carried out before the lateral spacers are formed, and consequently, the lateral spacers would extend down to the recessed surface, since only such a sequence of process steps would offset the double-diffused drain region from the gate structure as taught in document D1. A reverse process step sequence, as suggested by the appellant (cf. item V(b) above), would on the other hand result in a structure where the drain region is not vertically spaced from the gate insulation film. Such a structure would be contrary to the teaching of document D1 where it is specified that at least the drain region 3 should be separated from

the gate oxide layer 4, and thereby losing the main advantage of using a recessed structure (cf. D1a, page 5, lines 15 to 20, as well as all the Figures 4 to 6 where the drain region 3 is separated from the gate oxide layer 4).

- 2.6 For the above reasons, in the Board's judgment, the subject matter of claim 1 does not involve an inventive step within the meaning of Article 56 EPC. The application in suit therefore does not meet the requirements of Article 52(1) EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

L. Martinuzzi

The Chairman:

R. K. Shukla