BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS | BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE | CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [X] To Chairmen

D E C I S I O N
of 8 August 1997

Case Number: T 0054/95 - 3.4.1

Application Number: 90107998.8

Publication Number: 0395072

IPC: H01L 23/485

Language of the proceedings: EN

Title of invention:
Bonding pad used in semiconductor device

Applicant:
Kabushiki Kaisha Toshiba

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56, 84, 123(2)

Keyword:
"Disclosure, clarity and inventive step (after amendments: yes)"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0054/95 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 8 August 1997

Appellant: Kabushiki Kaisha Toshiba
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi
Kanagawa-ken 210 (JP)

Representative: Lehn, Werner, Dipl.-Ing.
Hoffmann Eitle
Patent- und Rechtsanwälte
Postfach 81 04 20
81904 München (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 15 September 1994 refusing European patent application No. 90 107 998.8 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. D. Paterson
Members: H. J. Reich
R. K. Shukla

Summary of Facts and Submissions

I. European patent application No. 90 107 998.8 (publication No. 0 395 072) was refused by a decision of the Examining Division.

II. The reason given for the refusal was that amended independent claims 1 to 5 filed 9 August 1993 comprise added subject-matter contrary to requirements of Article 123(2) EPC, and that the application does not meet the requirements of Article 84 EPC. In particular independent claim 5 does not contain essential features of the invention. The Examining Division also took the view that claim 1, even if it was clarified and properly based on the original disclosure, would not involve an inventive step in the sense of Article 56 EPC with regard to the prior art disclosed in documents

D1: US-A-4 613 956, and

D3: Patent Abstracts of Japan, volume 5, No. 181 (E-83)[853], 20 November 1981 relating to JP-A-56-108246

for the following reasons:

The subject-matter of claim 1 differs from the device disclosed in document D1 only in that the second conducting polycide level (38,40) is explicitly used as a bonding pad for bonding a wire thereon. The skilled person knows from document D3 that bonding pad structures are improved in their electrical and mechanical reliability by the provision of a multilayer structure of insulating and conducting layers below a bonding pad. On the other hand, it would be evident that the multilayer gate structure disclosed in document D1 has to be contacted from the outside, i.e.

by means of a bonding pad structure in another area of the semiconductor device. A skilled person who wishes to form in the device of document D1 not only electrode structures of improved integrity but also bonding pads of high electrical and mechanical quality, follows only his normal routine practice when forming the bonding pads with the same structure as used for the gate electrodes.

III. The appellant lodged an appeal against this decision, filed with the grounds of appeal a new amended set of claims 1 to 4 as a basis for grant and requested auxiliary oral proceedings.

IV. In a communication preparing for oral proceedings, the Board relied additionally on documents:

D2: US-A-4 426 764 and

D4: GB-A-2 206 234

cited also by the Examining Division, and informed the appellant of its provisional view that in the light of document D3 which teaches to improve the stability against bonding shocks by a bonding pad on top of additional poly-Si-layers, it may be obvious to use the particular bonding pad structure disclosed in document D4 in the semiconductor device according to document D1 and to arrive thereby at the essential subject-matter of independent claims 1 and 3.

V. Before the oral proceedings which were scheduled for the 17 July 1997, the appellant withdrew his former requests and requested grant on the basis of a new amended set of claims 1 to 6 filed on 17 June 1997.

Independent claims 1 and 4 filed on 17 June 1997 read as follows:

"1. A semiconductor device comprising:

(a) a semiconductor substrate (101);

(b) a first insulating layer (102) on said semiconductor substrate (101);

(c) an upper insulating layer (106) having a contact hole (107);

(d) a bonding pad (108) inside said contact hole (107);

(e.1) said bonding pad (108) including a metal electrode layer (110) to which a wire (118) is to be bonded

(e.2) and a barrier metal layer (109) underneath said metal electrode layer (110);

c h a r a c t e r i z e d i n t h a t

(f) said barrier metal layer (109) is arranged on a polycide layer (105);

(g.1) said polycide layer (105) is arranged on a second insulating layer (104);

(g.2) said second insulating layer (104) is a composite film constituted by oxide and nitride films;

(f) said second insulating layer (104) is arranged on a first polysilicon layer (103); and

(h) said first polysilicon layer (103) is arranged on said first insulating layer (102).

4. A semiconductor device comprising

(a) a semiconductor substrate (101);

(b) a first insulating layer (102) on said semiconductor substrate (101);

(c) an upper passivation layer (111) having a contact hole;

(d) a bonding pad (108) inside said contact hole;

(e.1) said bonding pad (108) including a metal electrode layer (110) to which a wire (113) is to be bonded

(e.2) and a barrier metal layer (109) underneath said metal electrode layer (110);

c h a r a c t e r i z e d i n t h a t

(f) said barrier metal layer (109) is arranged on a third polysilicon layer (120);

(g) said third polysilicon layer (120) is arranged on an interlevel insulator layer (106);

(h) said interlevel insulator layer (106) is arranged on a polycide layer (105);

(i.1) said polycide layer (105) comprises an upper metal silicide layer (105B)

(i.2) and a lower second polysilicon layer (105A);

(j.1) said lower second polysilicon layer (105A) is arranged on a second insulating layer (104),

(j.2) said second insulating layer (104) is a composite layer constituted by silicon oxide and silicon nitride films;

(k) said second insulating layer (104) is arranged on a first polysilicon layer (103); and

(l) said first polysilicon layer (103) is arranged on said first insulating layer (102)."

Claims 2 and 3 are dependent on claim 1 and claims 5 and 6 are dependent on claim 4.

VI. In support of this request the appellant argued essentially as follows:

(a) Independent claims 1 and 4 are delimited against the teaching of document D4 which discloses a two-layered bonding pad with a bottom layer of barrier metal. Since the device disclosed in document D4 is capable of performing the same function as the invention as claimed, and relates to the problem to be solved by the present invention, document D4 constitutes the closest prior art.

(b) The present invention is based on the recognition that the same layer systems which are commonly used for manufacturing the components of an EPROM, may also be used for providing a support structure for a bonding pad. Such use based on the

alternating soft-hard-soft mechanical properties of this layer system as disclosed in the original description page 4, lines 37 to page 5, line 11, would not be obvious in view of the cited prior art.

VI. With a fax dated 2 July 1997 the appellant was informed that the Board intended to allow the appeal, that oral proceedings scheduled for the 17 July 1997 were cancelled and that the appellant would receive a written decision in due course.

Reasons for the Decision

1. The features of claim 1 are disclosed in Figure 2 and the corresponding original description of this first embodiment, and the features of claim 4 are disclosed in Figure 3 and the corresponding original description of this second embodiment. Claims 2 and 5 are based on subject-matter disclosed in original claim 3 and Figures 2 and 3 showing that polycide layer 105 is present in both embodiments. The subject-matter claimed in claims 3 and 6 is disclosed in the original description page 4, line 37 to page 5, line 11. There is, therefore no objection under Article 123(2) to the current set of claims. In the Board's view, the wording of claims 1 to 6 is clear and the subject-matter of independent claims 1 and 4 comprises all essential features of the invention as set out in features (g.1) to (h) of claim 1 and in features (i.1) to (l) of claim 4. Hence, claims 1 to 6 are held to satisfy Article 84 EPC.

2. *Novelty - claims 1 to 4*

2.1 Document D4 only discloses the features defined by the identical wording of the pre-characterising parts of claims 1 and 4, i.e.:

A semiconductor device comprising: a semiconductor substrate (see D4, 12 in Figure 1e); a first insulating layer (20 in Figure 1e) on said semiconductor substrate; an upper insulating layer (42) having a contact hole (44); a bonding pad (40) inside said contact hole; said bonding pad including a metal electrode layer (34) to which a wire is to be bonded (D4, page 5 lines 4 to 8) and a barrier metal layer (36 of Ti, see D4, page 4, line 9 and the present application column 4, line 22) underneath said metal electrode layer.

2.2 In the closest prior art disclosed in document D4 bonding pad 40 is provided on top of a glass layer (26) serving as interlevel insulator and provided on a field oxide layer. None of the documents cited in the European Search Report discloses a device wherein a bonding pad is provided on top of the layer structure as defined in the characterising parts of independent claims 1 and 4.

2.3 Thus, the subject-matter of independent claims 1 and 4 is considered novel in the sense of Article 54 EPC.

3. *Inventive step - claims 1 and 4*

3.1 Claim 4 adds to the subject-matter of claim 1 a third polysilicon layer (120) on an interlevel insulator layer (106) directly under the bonding pad (108). The remaining subject-matter of both claims comprises the same technical starting point (see paragraph 2.1 above) and technically identical means within the

characterising parts of claim 1. Therefore, the question whether claims 1 and 4 involve an inventive step, can be answered for both claims by the same technical considerations.

3.2 Starting from the closest prior art device according to Figure 1e of document D4, the objective problem underlying claims 1 and 4 is to provide a semiconductor device which can prevent formation of a crack in an insulating oxide film when a wire is bonded to a bonding pad; see the description column 1, lines 53 to 56.

3.3 This problem is solved by the identical technical means defined in feature (g.1) to (h) of claim 1 and (i.2) to (l) of claim 4. In both claims the solution consists in a composite layer of oxide and nitride films which adjoins on each surface a polysilicon layer. This provision of the hard composite layer of oxide and nitride films between the soft polysilicon layers improves the mechanical strength between the bonding pad and the insulating oxide film to be protected.

3.4 Document D3 teaches to absorb and disperse shocks which occur during bonding by two polysilicon layers (5,7) each covered by a thin silicon oxide film (6,8). Since document D3 indicates explicitly that the silicon oxide layers are placed between bonding pad and substrate in order to decrease parasitic capacitances, it is clear to the skilled reader that this known solution is restricted to a shock absorber which is exclusively formed by polysilicon, i.e. by soft material.

3.5 Documents D1 and D2 wherein a system of polysilicon-oxide/nitride composite-polysilicon layers forms the control and floating gates of an EPROM, are totally silent about the mechanical resistance of these layers against pressure. Document D1, column 3, lines 22 to 39

teaches to use an oxide/nitride composite layer between two polysilicon gates because of its dielectric integrity and strength. Document D2, column 7, lines 9 to 19 suggests a skilled person to provide between two polysilicon gates an oxide/nitride composite, in particular an ONO-structure, i.e. a silicon nitride layer covered on both surfaces by silicon oxide films, in order to minimise strain caused by different coefficients of thermal expansion. Hence, there is no hint in the art of polysilicon gates of EPROMs insulated against each other by a composite oxide/nitride layer to any mechanically advantageous properties of such gate structure suggesting a use of this layer system as a shock absorber in order to avoid cracks of the underlying insulator of the semiconductor chip by impacts during bonding.

3.6 The above mentioned technical effects of the oxide/nitride composite as an interlayer between gates disclosed in documents D1 and D2, in the Board's view, do not allow a skilled person to recognise that not only an overall soft shock absorber as disclosed in document D3 but also a soft-hard-soft layer system represents a technical means which protects against cracks during bonding. In the Board's view it is not obvious to place a hard layer, i.e. the second insulating film (104) claimed, between two soft layers, i.e. to replace the conventional solution of an overall soft damping material (i.e. the cushion effect of document D3), by a material with a less deformable centre, which allows additionally for a local pressure distribution over the entire bonding pad area of impacts on the pad during bonding of the wire.

3.7 For the reasons set out in detail in paragraphs 3.2 to 3.6 above, the subject-matter of claims 1 and 4 is considered to involve an inventive step in the sense of Article 56 EPC.

4. Thus, claims 1 and 4 are allowable under Article 52(1), EPC. Dependent claims 2, 3, 5 and 6 concern particular embodiments of the device claimed in claim 1 or in claim 4 respectively and are, therefore likewise allowable.

5. The case is remitted to the Examining Division in order that the description should be adapted to the above set of claims.

Order

For these reasons it is decided that:

1. The decision of the Examining Division is set aside.

2. The case is remitted to the Examining Division with the order to grant a patent on the basis of claims 1 to 6 filed on 17 June 1997, with the description to be adapted accordingly.

The Registrar: The Chairman:

M. Beer G. D. Paterson