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D E C I S I O N
of 20 April 1999

Case Number: T 0357/95 - 3.4.3

Application Number: 89111233.6

Publication Number: 0347853

IPC: H01L 27/02, H01L 23/52, H04S 1/00

Language of the proceedings: EN

Title of invention:
Semiconductor integrated circuit

Applicant:
Sanyo Electric Co., Ltd.

Opponent:
-

Headword:
Semiconductor integrated circuit/SANYO ELECTRIC

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - yes (after amendments)"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0357/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 20 April 1999

Appellant: Sanyo Electric Co., Ltd.
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Moriguchi-shi, Osaka (JP)

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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 9 December 1994 refusing European patent application No. 89 111 233.6 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
M. J. Vogel

Summary of Facts and Submissions

I. European patent application No. 89 111 233.6 (publication No. 0 347 853) was refused in a decision of the Examining Division on the ground of lack of inventive step having regard to prior art documents D1: DE-A-2 017 607, D2: Proceedings of the IEEE 1985 Custom Integrated Circuits Conference, 20 to 23 May 1985, Portland, Oregon, USA, pages 68 to 71, and D3: Patent Abstracts of Japan, vol. 11, No. 179 (E-514), 9 June 1987 & JP-A-62 012147.

Claim 1, which was the only independent claim of the set of 24 claims forming the basis of the above decision, had the following text:

"1. A semiconductor integrated circuit comprising: a semiconductor chip (1), a plurality of layout areas (A to T) of substantially equal size formed on said semiconductor chip, each of said layout areas being capable of containing a plurality of circuit elements (10 to 13) , partition regions (4) arranged between adjacent layout areas for separating said layout areas (A to T) from each other, and a pair of supply lines consisting of one power line (2) and one ground line (3) provided on each of said partition regions (4), an electronic circuit formed on said semiconductor chip including circuit blocks having different circuit configurations and circuit functions, said circuit blocks being designed by using each of said layout areas (A to T) as a unit, said plurality of circuit elements in a layout area being smaller than the number

of circuit elements of at least one circuit block such that said at least one circuit block is constituted by a group of two or more layout areas, wherein in each group of layout areas only one circuit block is arranged."

The arguments forming the basis of the decision can be summarized as follows:

The semiconductor integrated circuit known from D1 comprises a semiconductor chip with a plurality of layout areas of equal size, each being capable of containing a plurality of circuit elements, with partition regions arranged between adjacent layout areas, and with a pair of supply lines consisting of one power line and one ground line provided on each of said partition regions. In this large scale integrated (LSI) circuit, the layout areas are used as units to design any electronic circuit on the chip.

In relation to the above prior art, the objective problem underlying the claimed subject-matter was to realise complex circuits which had functional blocks requiring more circuit elements than could be accommodated within one layout area. This problem was a common incentive for a person skilled in the art of designing LSI circuits. Thus, the problem itself did not contribute to an inventive step, especially since D1 (see the sentence bridging pages 8 and 9) explicitly points out the possibility of forming any LSI circuit in the layout areas.

In view of the information in D1, it would be immediately obvious to apply the known concept of basic

circuits constituted by layout areas of equal size to the design of complex LSI circuits consisting of a plurality of circuit blocks of different configuration and function.

Should the skilled person have had the slightest doubt whether integrated circuits formed of circuit blocks of different configuration and function can be formed from basic units or layout areas of equal size, he would have found an example in D3, which showed a tuner circuit formed from a plurality of layout areas of equal size arranged in groups of four to form circuit blocks. D2 was also a relevant document for the arrangement of circuit blocks.

Therefore, the subject-matter of claim 1 lacks an inventive step.

II. The applicant lodged an appeal against this decision and filed amendments with the statement of the grounds of appeal dated 18 April 1995, whereby in particular lines 23 to 25 of original page 27 and original page 28 were deleted.

III. During the oral proceedings held on 20 April 1999, the appellant (applicant) filed a new set of 24 claims and amendments for page 3 of the description, and requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: Nos. 1 to 24, submitted in the oral proceedings;

Description: Pages 1, 2 and 4 to 26 as originally filed;
Page 3, as originally filed, but incorporating the amendments submitted during the oral proceedings, i.e. with the cancellation of lines 6 to 22 and replacement by pages 1 and 2 of the text submitted during the oral proceedings;
Page 27, as originally filed, but with the amendment requested in the appellant's letter dated 18 April 1995, i.e. with the cancellation of lines 23 to 25 thereof;

Drawings: Sheets 1/14 to 14/14, as originally filed.

Claim 1 is the only independent claim and reads as follows:

"1. A semiconductor integrated circuit comprising: a semiconductor chip (1), a plurality of layout areas (A to T) of substantially equal size formed in said semiconductor chip, each of said layout areas being capable of containing a plurality of circuit elements (10 to 13), partition regions (4) arranged between adjacent layout areas for separating said layout areas (A to T) from each other, and a pair of supply lines consisting of one power line (2) and one ground line (3) provided on each of said partition regions (4), an electronic circuit formed in said semiconductor chip, characterized in that said electronic circuit includes circuit blocks each comprising an analog circuit having different circuit configurations and circuit functions,

said circuit blocks being designed by using each of said layout areas (A to T) as a unit, said layout areas containing a preferable number of circuit elements according to circuit blocks incorporated in said semiconductor chip such that a plurality of said circuit blocks are constituted by groups of two or more layout areas, wherein in each group of layout areas only one circuit block is arranged."

V. The appellant (applicant) has submitted essentially the following arguments in support of his request:

Claim 1 is now drafted with a pre-characterizing portion corresponding to the content of D1 and specifies *inter alia* that each of the circuit blocks comprises an analog circuit having different circuit configurations and circuit functions; moreover, it defines more precisely the structure of the semiconductor chip with said layout areas containing a preferable number of circuit elements according to circuit blocks incorporated in said semiconductor chip such that a plurality of said circuit blocks are constituted by groups of two or more layout areas, wherein in each group of layout areas only one circuit block is arranged.

The amendments in claim 1, in the dependent claims and in the description are based on the original disclosure, and they meet all the objections raised in the impugned decision.

Novelty of the invention as claimed has not been disputed in the decision under appeal.

In the semiconductor integrated circuit known from D1, the electronic circuit is a LSI circuit and includes circuit blocks each comprising a circuit having the same circuit configurations and circuit functions, in particular a digital or logic circuit having a logic function. In D1, there is no explicit information about analog circuits and, therefore, no indication about circuit blocks each comprising an analog circuit having different circuit configurations and circuit functions. Moreover, it is not derivable from D1 that the circuit blocks are designed by using each of said layout areas as a unit, said layout areas containing a preferable number of circuit elements according to circuit blocks incorporated in said semiconductor chip such that a plurality of said circuit blocks are constituted by groups of two or more layout areas, wherein in each group of layout areas only one circuit block is arranged.

The problem underlying the present invention is the one mentioned in the application, i.e. to simplify changes in the design of "custom" integrated circuits in accordance with the requirements of a user, and this problem is not addressed by D1 or D3.

Integrated circuits formed of circuit blocks of different configurations and functions formed of basic units or layout areas of equal size are known from D3. However, these circuit blocks are shielded from each other in respective basic units and are therefore not designed with a preferable number of circuit elements according to the circuit blocks, as in the present claim 1. The solution offered by D2 would lead to layout areas having different sizes and shapes, and

consequently having the drawbacks of the prior art mentioned in the description of the present application with respect to changes in the arrangement of these areas.

Therefore, starting from D1, the subject-matter of present claim 1 is not obvious to the person skilled in the art and thus involves an inventive step.

Reasons for the Decision

1. The appeal is admissible.

2. *Admissibility of the amendments*

In the decision under appeal, claim 1 forming the basis of the decision was considered to comply with the requirement of Article 123(2) EPC. Present claim 1 differs from the above claim in that it specifies that the circuit blocks are all analog circuits and in that the layout areas and the circuit blocks are defined clearly.

The dependent claims have been amended for clarity and consistency with the description.

The Board is satisfied that the amendments meet the requirement of Article 123(2) EPC. Also in the Board's view the amended claim complies with the requirements of Article 84 EPC.

3. The only issue under dispute in the present appeal is that of inventive step.

3.1 A semiconductor integrated circuit is known from D1 (see in particular Figures 1 to 4 and 6 to 8 with the corresponding description, and page 2, second paragraph), which comprises:

a semiconductor chip (10), a plurality of layout areas (20a to 20g) of substantially equal size formed in said semiconductor chip, each of said layout areas being capable of containing a plurality of circuit elements such as transistors and resistors;

partition regions arranged between adjacent layout areas for separating said layout areas (20a to 20g) from each other, and

a pair of supply lines (32, 31) consisting of one power line (32) and one ground line (31) provided on each of said partition regions, and

an electronic circuit formed in said semiconductor chip.

However, in this known semiconductor integrated circuit, which corresponds to the pre-characterising portion of the present claim 1, the electronic circuit is a LSI-circuit, i.e. a large scale integrated circuit and includes circuit blocks each comprising a circuit having the same circuit configurations and circuit functions, in particular a digital or logic circuit having a logic function (see page 1, first paragraph to page 2, first paragraph).

Indeed, as set forth in the impugned decision (see the second paragraph of point 3.2 of the reasons), it can

be derived from the sentence bridging pages 8 and 9 of D1 that the circuit block ("Einheitszelle") of the LSI circuit needs not be the one shown in Figure 4. However, D1 contains no explicit indication that circuits are analog circuits.

In the semiconductor integrated circuit according to the claimed invention, on the other hand, the electronic circuit includes circuit blocks each comprising an analog circuit having different circuit configurations and circuit functions. Moreover, in contrast to the circuit known from D1, the circuit blocks are designed by using each of said layout areas as a unit, the layout areas containing a preferable number of circuit elements according to circuit blocks incorporated in said semiconductor chip such that a plurality of the circuit blocks are constituted by groups of two or more layout areas, wherein in each group of layout areas only one circuit block is arranged.

3.2 Starting from D1 and taking into account the present text of claim 1, the problem underlying the present invention thus concerns the formation of analog circuits in a chip.

Integrated circuits formed of circuit blocks of different configurations and functions formed of basic units or layout areas of equal size are known from D3 (see the abstract); however, these circuit blocks are shielded from each other in respective basic units and there is no disclosure in D3 that each of the circuit blocks is constituted by a group of two or more layout areas of equal size, as in the present claim 1.

The solution offered by D2 would lead to circuit blocks having different sizes and shapes, and consequently having the drawbacks of the prior art mentioned in the description of the present application, i.e. of considerable time and costs when modifying and rearranging the design of an integrated circuit in accordance with the requirements of a user.

3.3 Therefore, having regard to the state of the art, the subject-matter of present claim 1 is not obvious to a person skilled in the art, so that it involves an inventive step in the sense of Article 56 EPC.

4. Consequently, claim 1 is patentable in the sense of Article 52(1) EPC, so that a patent can be granted on this basis (Article 97(2) EPC).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the following documents:

Claims: 1 to 24 submitted in the oral proceedings dated 20 April 1999;

Description: Pages 1, 2, 4 to 26 as originally filed;
Page 3 as originally filed, but

incorporating the amendments as submitted on pages 1 and 2 at the oral proceedings;
Page 27, as originally filed, but with the amendment requested in the appellant's letter dated 18 April 1995;

Drawings: Sheets 1/14 to 14/14, as originally filed.

The Registrar: The Chairman:

D. Spigarelli R. Shukla