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D E C I S I O N
of 13 August 1997

Case Number: T 0760/95 - 3.5.2

Application Number: 91109162.7

Publication Number: 0463418

IPC: H03L 7/18

Language of the proceedings: EN

Title of invention:
A broad operational range, automatic device for the change of frequency in the horizontal deflection of multisynchronization monitors

Applicant:
SGS-THOMSON MICROELECTRONICS s.r.l.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - yes; after amendment"

Decisions cited:
-

Catchword:
-

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Case Number: T 0760/95 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 13 August 1997

Appellant: SSG-THOMSON MICROELECTRONICS s.r.l.
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Decision under appeal: Decision of the Examining Division of the European Patent Office posted 28 March 1995 refusing European patent application No. 91 109 162.7 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: A. G. Hagenbucher
B. J. Schachenmann

Summary of Facts and Submissions

I. The present appeal contests the decision of the examining division refusing the appellant's European patent application No. 91 109 162.7.

II. The reason given for the refusal was that the subject-matter of claim 1 then on file did not involve an inventive step having regard to

D1: US-A-4 399 459 and
D2: DE-A-3 708 538.

III. In response to a communication from the board the appellant filed new claims and amendments to the description.

IV. Independent claim 1 is now worded as follows:

"1. A broad operational range, automatic device for the change of frequency in the horizontal deflection of a multi-synchronization monitor, comprising an integrated circuit (2) incorporating,

a connection for receiving an analog synchronization signal (S1) having said frequency on a circuit input;

a phase comparator (14) having two inputs (15,16) and receiving said synchronization signal (S1) on one (15) of said two inputs (15,16);

a voltage controlled oscillator (12) adapted to generate at its output (11) a signal (S3) having a frequency depending on a voltage (Vc) applied at an input (13) thereof which is linked operatively to an output (22) of said phase comparator (14);

a counter (9) having a first input (10) connected to said oscillator (12) output (11) and an output (21) connected to the other input (16) of said phase

comparator inputs (15, 16) and being operative to generate at its output (21) a signal (S3/N) having a frequency equal to the division of the frequency of the output signal (S3) from the oscillator (12) by a division factor (N);

characterized in that said integrated circuit comprises a frequency meter (3) connected to said circuit input for receiving said analog synchronization signal (S1) and operative to generate a numerical value (N) corresponding to the frequency of said synchronization signal at one output and in that said counter (9) has a second input linked operatively to the meter (3) output (5) for receiving said numerical value (N) corresponding to the frequency of the synchronisation signal (S1) to be used as the counter division factor, said counter output (21) being connected to the integrated circuit output."

Claims 2 to 4 are dependent on claim 1.

V. Considering also the comments presented during the examining proceedings the appellant essentially argued as follows:

Conventional monitors normally operated at a predetermined fixed horizontal deflection frequency. A video signal to be displayed comprised a synchronization (sync) signal, the frequency of which equalled the monitor predetermined horizontal deflection frequency. An oscillator having a free-running frequency near the horizontal deflection frequency was usually provided for generating the horizontal deflection signal. The frequency and phase of the oscillator output were controlled by a phase-locked loop (PLL) to match the frequency and phase of the sync signal.

The object of the invention was to provide a circuit for generating a horizontal deflection signal, the frequency of which was not fixedly predetermined, but could vary automatically to match any sync frequency within a broad range (10-100kHz).

The circuit according to the invention, as defined in claim 1, used a PLL in which the voltage controlled oscillator (VCO:12) had a frequency much higher than the typical frequency of a horizontal deflection signal. The circuit comprised means (3) for measuring the frequency of the sync signal (S1) as a numerical value (N) and means (9) for dividing the oscillator output frequency by the numerical value (N) of the measured frequency. The signal (S3/N) resulting from the division was compared with the sync signal (S1) in the phase comparator (14) of the PLL. The output (Vc') from the comparator (14) was used for adjusting the oscillator frequency so that the division of the frequency by N equalled the sync frequency. The signal (S3/N) resulting from the division was used for controlling the horizontal deflection.

Document D1 disclosed a circuit for accepting horizontal and vertical frequency input signals having frequencies variable over a wide range for generating a composite video sync signal in accordance with the NTCS standard. The circuit comprised a PLL (32, 40, 42) which included a frequency divider (42). The frequency divider divided the frequency from the voltage controlled oscillator (VCO (40)) by a predetermined number and generated four signals having different phases which were suitably processed to obtain the desired composite video sync signal.

The circuit known from document D1 did not have the following features of the device according to claim 1:

- a frequency meter receiving the analog sync signal and generating a numerical value corresponding to the frequency of said sync signal and

- the counter division factor being predetermined by the measured numerical value.

Document D2 disclosed an oscillator which generated a signal having a frequency controllable with high accuracy and high rapidity. The oscillator comprised a PLL with a frequency divider (5), an arrangement (26) for measuring the difference between a frequency related to the frequency (fR) of a signal for controlling the PLL and a reference frequency (fM/y) and a unit (22) which could provide to the frequency divider (5) a signal to change the division factor and thus the oscillator output frequency (fA).

D2 did not disclose a frequency meter which received a sync signal and generated a numerical value corresponding to the frequency of the sync signal. It did not suggest using a numerical frequency measure as a division factor for a programmable divider. Furthermore, the oscillator output was derived from the VCO output and not from the divider (5) output. The circuit according to D2 should improve lock-time and adjustment accuracy, while the claimed circuit used a frequency meter and a programmable counter with a completely different object, as explained above.

The statement in section 2(d), last but one paragraph of the impugned decision was incorrect because document D2 did not suggest that the output of the

differential frequency meter 26 could be used to set the division factor of the divider 5. It appeared that the division factor n of divider 5 was determined by the microprocessor 22 to provide a coarse frequency adjustment, for example in frequency steps.

The frequency measure obtained through the arrangement 26 had nothing to do with the division factor n. A differential frequency measure of the input signal for a PLL was used by the microprocessor 22 to calculate a parameter (Z_{SOLL}) related to the desired oscillator frequency (f_1) and to provide a digital signal to the digital-to-analog converter 20 to obtain a fine adjustment (via 14 and 12) of the oscillator frequency within the frequency range of a frequency step.

In view of these differences D2 in combination with D1 did not render the subject-matter of present claim 1 obvious.

VI. The appellant requested that the decision of the examining division be set aside and a patent be granted on the basis of the following documents:

Claims: 1 to 4 as filed with the letter of 24 July 97, received 29 July 1997;

Description: pages 4 to 6, 8 as originally filed; pages 1, 2, 2a, 3, 7 as filed with the letter of 24 July 97;

Drawings: sheets 1/2 to 2/2 as originally filed.

Reasons for the Decision

1. The appeal is admissible.

2. The amendments made to the documents (claims and description) comply with the requirements of Article 123(2) EPC. All the features in present claim 1 can be found in original claims 1 and 5 and in the description of figure 1 on pages 4 to 7 of the originally filed description. The dependent claims are based on the originally filed dependent claims and the description of figure 1.

3. None of the cited documents D1 or D2 discloses all the features of the subject-matter defined in present claim 1. Since novelty is not in dispute, the issue to be decided is whether the subject-matter of claim 1 is objectionable for lack of inventive step.

4. *Closest prior art and problem:*

The closest prior art is the flexible video synchronization circuit shown in D1. This circuit has all the features indicated in the preamble of claim 1, namely a PLL comprising a phase comparator 32, a voltage controlled oscillator 40 and a divide-by-fourteen digital frequency divider 42 receiving a variable horizontal frequency input signal - see D1, figure 2. The frequency divider provides the output signal of the PLL and has a fixed and predetermined division ratio. Four signals having different phases are generated which are suitably processed to obtain the desired composite video synchronization signal,

specified in NTSC standard. Technological developments require, however, recurrent changes in the working frequencies for horizontal deflection, eg due to new standards, to be implemented without a great number of discrete components in the PLL.

The problem underlying the subject-matter of claim 1 may therefore be seen in the provision of a circuit with the features in the preamble of claim 1, which has such structural and functional features as to enable continuous and stable synchronization through a broad frequency range, e.g. between 10 and 100kHz.

5. This problem is essentially solved by providing a counter with a settable division factor, which is determined by a meter according to the measured frequency of the inputted synchronisation signal as specified in the characterising part of claim 1. As explained in the description (page 7, 4th paragraph and page 8, 2nd paragraph) it is the settable counter which makes it possible to extend the input frequency range whilst retaining a stable operation because of a high VCO oscillator frequency.

6. There is no hint in the available prior art to vary the division factor in the counter of D1 in accordance with the frequency of the input signal.

Document D2 discloses an oscillator circuit comprising a digital PLL 1 with a VCO 2 providing the output signal of the PLL. The frequency of the output signal is hence only dependent on the control voltage received by the VCO. A settable frequency divider 5 receives this output signal and provides the input signal for a phase comparator 10 which compares it with a nearly constant reference frequency f_{RZ} . An output frequency range can thus be coarsely selected by the division factor. The reference frequency is stabilised and

adjusted for fine-tuning of the output signal in a control loop comprising a differential frequency meter 26 which substantially compares the reference frequency with a frequency standard f_M - see D2, page 3, lines 38 to 42 and 47 to 53; page 5, lines 44 to 51. No link between this control loop and the division factor of the settable divider 5 of the PLL 1 can, however, be found in D2.

7. Moreover, the problem solved by D2 differs substantially from the problem solved by the present invention. The present invention seeks to track an input signal with a variable frequency which may vary in a broad range, whereas D2 seeks to provide an output frequency which varies in a broad range whilst the reference input frequency is nearly constant and only fine-tuned.

8. The board, therefore, comes to the conclusion that the subject-matter of claim 1 cannot be derived in an obvious manner from the documents cited by the examining division in the decision under appeal. The further documents cited in the European search report are not more relevant than documents D1 and D2. Claim 1 must accordingly be seen as involving an inventive step as required under Articles 52(1) and 56 EPC.

9. In the opinion of the board, independent claim 1, together with dependent claims 2 to 4 are allowable. The description has been adapted to the wording of the claims and meets the requirements of the EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent in the form requested by the appellant (see paragraph VI above).

The Registrar:

M. Kiehl

The Chairman:

W. J. L. Wheeler