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D E C I S I O N
of 2 October 2000

Case Number: T 0972/95 - 3.4.3

Application Number: 90310818.1

Publication Number: 0423973

IPC: H01L 21/90

Language of the proceedings: EN

Title of invention:
Silicide gate level runners

Applicant:
AT&T Corp.

Opponent:
-

Headword:
Selectively increasing the conductivity/AT&T

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes)"
"Interpretation of the term "selective" in prior art document"

Decisions cited:
-

Catchword:

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0972/95 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 2 October 2000

Appellant: AT&T Corp.
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Representative: Watts, Christopher Malcolm Kelway, Dr.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 23 May 1995 refusing European patent application No. 90 310 818.1 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
M. J. Vogel

Summary of Facts and Submissions

I. European patent application No. 90 310 818.1 was refused by the decision of the examining division dated 23 May 1995 on the ground that the application did not comply with the requirements of Article 52(1) EPC, since the subject matter of claim 1 filed with the letter dated 10 January 1995 did not involve an inventive step.

In the examination procedure, following prior art documents were cited:

D1: Journal of Vacuum Science and Technology, vol. 17, pages 775-792 (1980);

D2: IBM Technical Disclosure Bulletin, vol. 31, no. 7, December 1988, page 154; and

D3: EP-A-0 285 410.

II. The appellant (applicant) lodged an appeal on 19 July 1995, payed the appeal fee on 14 July 1995, and filed a statement of the grounds of appeal on 22 September 1995.

III. In response to a communication from the Board, the appellant filed with a letter dated 10 April 2000, a new claim 6 together with page 2A of the description. The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: Nos. 1 to 5 as filed with the letter dated 10 January 1995

No. 6 as filed with the letter dated 10 April 2000

Description: Pages 1 to 4 as originally filed
Page 2A as filed with the letter dated 10 April 2000

Drawings: Sheet 1/1 as originally filed.

IV. Claim 1 of the above request reads as follows:

"A method of fabricating integrated circuits comprising the steps of:

depositing a layer of a conducting material on a substrate (1) which includes field oxide regions (13) and device regions;

patterning said conducting material on said field oxide regions (13) to form conductive runners (17) and a gate structure (3) on said substrate (17) surface comprising a conductive material (7);

forming a first dielectric (15) over said substrate (1) which covers said conductive runners (17) and said gate structure (3);

etching back said dielectric (15) to expose the top surfaces of said conductive runners (17) on said field oxide regions (13) but not said gate structure (3) on said device regions; and

increasing the conductivity of said exposed conductive runners (17)."

V. In the decision under appeal, the examining division argued essentially as follows:

(A) Document D1 discloses that silicide on polysilicon interconnect lines enables the reduction of the

resistance and the preservation of the polysilicon gate in MOS devices. Furthermore, document D1 mentions on page 781 that selective silicidation of exposed silicon (polysilicon) areas represents a real advantage. As the use of polysilicon as gate electrodes and interconnects is fully conventional in the art, the skilled person would derive from the teaching of D1 that polysilicon gates and interconnects can be provided selectively with silicide to increase the conductivity of predetermined areas.

(B) Starting from document D1, the objective problem related to fabricating an integrated circuit having a planar surface despite having field oxide regions.

(C) Since the features distinguishing the claimed invention from document D1 are known from document D3, the skilled person faced with the task of fabricating an integrated circuit having a planar surface and field oxide regions would readily recognize that the method of document D3 would enable the exposure of conductive runners for selective silicidation while maintaining protected structures formed in the active device regions.

VI. In the statement of grounds of the appeal, the appellant argued essentially as follows:

(a) Document D1 does not teach a process that would permit one to obtain a thicker silicide layer on a polysilicon runner than on the source/drain region, for example. Moreover, the passage on page 781 of document D1 seems to refer to a

conventional technique for creating a silicide within a window, presumably over a source/drain region.

(b) Neither document D1 nor D3 show any appreciation of one of the problems solved by the applicant, i.e. that a thick silicide may be desirable over a polysilicon runner, but not on the source/drain regions (cf. application, page 1, line 28 ff). Thus, the problem formulated by the examining division in its decision is incorrect.

(c) Document D3 is primarily concerned with a method for forming metal interconnects, in particular the planarization of metal pillars and is therefore not related to the technical field of document D1 (cf. D3, column 1, lines 27-37).

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Amendments*

Claim 6 and page 2A were amended in the appeal procedure for consistency with the wording of claim 1 and to comply with Rule 27(1)(b) and (c) EPC. The amendments also meet the requirements of Article 123(2) EPC.

3. *Inventive step*

The only issue in the present appeal is that of

inventive step.

2.1 Document D1, which is considered as the closest prior art, is a review article on the use of silicides in VLSI circuits, in particular for reducing the resistivity of polysilicon gates and interconnects (cf. page 775, "I. Introduction"). The document describes various methods of forming silicides by sintering a thin film metal-silicon composite (cf. section III "Formation of the silicides" on page 780 ff). A method of forming silicide on desired areas of a wafer using a patterned mask is described on page 781, paragraph bridging both columns. It follows from this description that according to this method, desired areas of a silicon substrate are exposed by openings in a mask on the wafer. A metal layer is deposited on the entire wafer, and during the subsequent heating step, metal silicide forms only where the metal is in contact with silicon. The metal which has not reacted with silicon is etched away in an etch which reacts only with the metal and does not react with the masking material, leaving silicide on the desired locations.

It is furthermore mentioned in document D1 that silicides can be used as a gate metal either directly on the gate oxide or on the polysilicon gate (cf. D1, page 787, left hand column, lines 7 to 10).

2.2 Document D1 is only concerned with the use of silicides in processes of fabricating integrated circuits, such as VLSI circuits, and does not disclose any of the further process steps required for fabricating an integrated circuit. In particular, the step of selectively increasing the conductivity of the conductive runners on the field oxide regions, but not

of the gate structure, is not disclosed in document D1.

2.2.1 According to the decision under appeal, document D1 disclosed selective silicidation of exposed silicon (polysilicon) areas, so that there was a clear teaching in document D1 that polysilicon gates and interconnects in conventional MOS devices can be subjected to selective silicidation to increase the conductivity of predetermined areas thereof (cf. item V(A) above).

2.2.2 The Board however agrees with the appellant's submission that the statement on page 781 of document D1 relates to the technique of forming silicide within windows in a mask made of silicon oxide exposing silicon regions. Selective silicidation in document D1 is thus not concerned with silicidation of selected portions of a conductive pattern comprising conductive runners and a gate structure, as in the claimed invention.

2.3 Document D2 discloses a process where self-aligned silicide regions are formed on the gate electrodes and the source/drain regions of a CMOS integrated circuit in two separate silicidation steps. The purpose of this process is to allow the silicide layers on the source and drain regions to be thinner than on the gate electrodes. The method comprises the step of forming cobalt silicide on the source and drain regions while masking the gate electrodes. After removing the mask, titanium is deposited which, during the sintering step, reacts with silicon to form titanium silicide only on the gate electrodes, since cobalt silicide on the source and drain regions prevents titanium from reacting with silicon.

There is no disclosure in document D2 concerning conductive runners on the field oxide regions separating the active device.

2.4 Document D3 is concerned with the formation of metal interconnect on MOS integrated circuits where field oxide regions are used to isolate the active devices from each other, i.e. a substrate with uneven surface. In the disclosed embodiment, a gate conductive runner formed on a field oxide region and a contact region in the semiconductor substrate are both interconnected to a wiring layer via metal pillars 30, 32 (cf. Figure 1; column 3, lines 24 to 37). The method disclosed in document D3 features metal pillars formed of a laminated metal structure having an intermediate etch stop layer. By etching down a dielectric layer with planar surface to expose and etch the highest metal pillars, a structure is obtained where all the metal pillars have identical elevations.

Document D3 however neither discusses the use of silicides nor any other means to increase the conductivity of polysilicon components, such as gate conductive runners, of the integrated circuit.

2.5 The technical problem, as stated in the application as filed, relates to the observation that a thick silicide layer in the gate induces high stress in the underlying gate oxide layer or that some silicide may penetrate the gate oxide layer, and thereby adversely affecting the device characteristics. Similarly, a thick silicide layer on source and drain regions might destroy the source/drain regions. On the other hand, the resistivity of the conductive runners providing the interconnection between neighboring devices of an

integrated circuit should be reduced as the cross-sectional area of the conductive runners decreases, thereby requiring a thick layer of silicide or metal on the conductive runners (cf. page 1, line 30 to page 2, line 11).

Also, having regard to the features distinguishing the claimed invention from the closest prior art document D1, the objective technical problem addressed by the present invention is the one as set out in the application as filed (cf. item above), i.e. to improve the overall conductivity of a conductive pattern in an integrated circuit device without adversely affecting the device characteristics.

2.6 As discussed above, the statement on page 781 of document D1 regarding the formation of silicides "only in selected areas" and relied upon in the decision under appeal, only refers to the method of forming silicide within a window.

Although document D1 discusses the presence of tensile stress in silicide films, this problem is reduced by an appropriate choice of metals, using higher sintering temperatures and/or using a cosputtering of silicide (cf. D1, pages 785 to 786, Section III B, "Stress in the silicide films"). It even appears from reading document D1 that the tensile stress can be reduced to such a degree that a gate electrode made entirely of silicide is not ruled out (cf. page 787, left hand column, lines 7 to 10; page 775, right hand column, second paragraph, last sentence; page 790, right hand column, last sentence).

Thus, the Board agrees with the submissions made by the

appellant that there is no appreciation in document D1 that the silicide (if any) on the gate electrode should be thinner than that on the conductive runner. On the contrary, a layer of silicide on the gate electrodes is described as desirable.

The skilled person therefore does not get any hint regarding the silicidation of conductive runners only with a view to preventing any adverse effect on the device characteristics.

2.7 Document D2 teaches that the thickness of the silicide layers on the source and drain regions should be kept thin, but the method of document D2 produces a thicker silicide layer on the gate electrodes than the silicide formed on the source and drain regions. Consequently, the skilled person would not get any help here for arriving at the claimed method where the conductive runners, and not the gate structure, undergo a conductivity increasing treatment.

2.8 For the foregoing reasons, in the Board's judgement, the subject matter of claim 1 involves an inventive step as required by Article 52(1) EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance to grant a patent on the basis of the documents as specified under item III above.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla