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DECISION of 8 August 2001

Case Number:

T 0712/96 - 3.4.3

Application Number:

90116251.1

Publication Number:

0414257

IPC:

H01L 23/495

Language of the proceedings: EN

Title of invention:

Resin sealing type semiconductor device in which a very small semiconductor chip is sealed in package with resin

Applicant:

KABUSHIKI KAISHA TOSHIBA

Opponent:

Headword:

Printed circuit board/TOSHIBA

Relevant legal provisions: EPC Art. 84, 56

Guidelines C-III, 4.2

Keyword:

"Reading a claim with an attempt to make technical sense out of

Decisions cited:

Catchword:



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Boards of Appeal

Chambres de recours

Case Number: T 0712/96 - 3.4.3

DECISION of the Technical Board of Appeal 3.4.3 of 8 August 2001

Appellant:

KABUSHIKI KAISHA TOSHIBA

72, Horikawa-cho Saiwai-ku

Kawasaki-shi

Kanagawa-ken 210 (JP)

Representative:

Lehn, Werner, Dipl.-Ing.

Hoffmann Eitle

Patent- und Rechtsanwälte

Postfach 81 04 20 D-81904 München

Decision under appeal:

Decision of the Examining Division of the European Patent Office posted 18 March 1996 refusing European patent application

No. 90 116 251.1 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman:

M. Chomentowski

Members:

G. L. Eliasson

P. H. Mühlens

Summary of Facts and Submissions

I. European patent application No. 90 116 251.1

(publication No. 0 414 257) was refused in a decision of the examining division dated 18 March 1996. The ground for the refusal was that the subject matter of the claims according to the submitted requests did not involve an inventive step having regard to the prior art documents

D5: EP-A-0 247 775;

D2: EP-A-0 247 644; and

D4: Patent Abstracts of Japan, vol. 10, No. 158 (E-409) [2214], 6 June 1986 & JP-A-61 014 731.

- II. Claim 1 is the only independent claim of the main request under consideration in the decision under appeal. It reads as follows:
 - "1. A moulded material type semiconductor device for sealing a very small semiconductor chip (32) in a package, having a plurality of electrodes (35) arranged on a surface of the semiconductor chip (32), comprising:

a bed (31) having a surface on which said semiconductor chip (32) is mounted, said surface having a peripheral surface portion extending beyond the periphery of said semiconductor chip (32);

a plurality of leads (34) surrounding said bed
(31);

a printed circuit board (33) having a wiring pattern thereon having first and second ends (36, 38), provided between said semiconductor chip (32) and said leads (34);

first connecting means (37) connecting the electrodes (35) on said semiconductor chip (32) to the first end (36) of the wiring pattern on the surface of said printed circuit board (33);

second connecting means (39) connecting said leads (34) to the second end (38) of the wiring pattern on the surface of said printed circuit board (33); and

moulded material (40) covering said semiconductor device with parts of said leads (34) left uncovered;

said moulded material (40) being moulded resin; said printed circuit board (33) having an underside surface portion at an inner side of the printed circuit board (33), said underside surface portion being part of the opposite surface of said printed circuit board (33) to that having said first connecting means (37) arranged thereon, and overlapping and being fixed to said peripheral surface portion of the bed (31) surrounding said semiconductor chip (32) without contact between said printed circuit board (33) and said chip (32); and

said first connecting means being bonding wires (37) and said second connecting means being TAB tape (39)."

- III. The reasoning of the examining division in the decision under appeal can be summarized as follows:
 - (a) Document D5 discloses a chip package device comprising a chip 20 attached to a bed 13 and a leads 11 of a lead frame (cf. Figures 2 and 3). A TAB tape 17 with conductive fingers 16 is positioned between the lead frame and the chip.

The conductive fingers are bonded to the leads 11 of the lead frame on one side, and are connected to the chip 20 via bonding wires 22. The chip and lead frame are encapsulated in e.g. an epoxy or plastic molding compound.

- (b) The TAB tape 17 having a wiring pattern 16 known from the device of document D5 was considered to fall under the term "printed circuit board" in claim 1. Thus, the device of claim 1 according to the main request differs from that of document D5 only in that the connection between the circuit board and the leads is established using a TAB tape, whereas in document D5 it is through direct bonding. Since there are only three basic methods of bonding (direct bonding, wire bonding and TAB bonding), the above difference was merely seen to be a conventional alternative.
- IV. The appellant (applicant) lodged an appeal on 13 May 1996, paying the appeal fee the same day. A statement of the grounds of appeal was filed on 17 July 1996.
- V. At the oral proceedings held on 8 August 2001, the appellant requested that the decision under appeal be set aside and a patent be granted on the basis of:

Claims: 1 to 4 filed during the oral proceedings of 8 August 2001;

Description: pages 3a and 4, filed during the oral proceedings of 8 August 2001, pages 1 and 5 to 8 filed with the letter dated 3 January 1996, page 2 as originally filed;

Drawings: Figures 1 to 8 as originally filed.

VI. Claim 1 according to the appellant's request differs from claim 1 under consideration in the decision under appeal only in that "first connecting means (37)" in the penultimate paragraph is replaced by "wiring pattern".

Independent claim 4 according to the appellant's request reads as follows:

"4. A moulded material type semiconductor device for sealing a plurality of very small semiconductor chips (55-61) in a package, having a plurality of electrodes (67) arranged on a surface of the semiconductor chip (55-61), comprising:

a plurality of beds (51-54) each having a surface on which at least one of said semiconductor chips (55-61) is mounted, said surface having a peripheral surface portion extending beyond the periphery of said semiconductor chip (55-61);

a plurality of leads (66) surrounding said plurality of beds (51-54);

a plurality of printed circuit boards (62-65) each having a wiring pattern thereon having first and second ends, provided between said semiconductor chip (55-61) and said leads (66);

bonding wires (69) connecting the electrodes (67) on each of said semiconductor chips (55-61) to the first end (68) of the wiring pattern on the surface of the corresponding printed circuit board (62-65);

TAB tape (71) connecting said leads (66) to second ends of the wiring pattern on the surface of said printed circuit boards (62-65); and

moulded material (81) covering said semiconductor device with parts of said leads (66) left uncovered;

said moulded material (81) being moulded resin;

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each of said printed circuit boards (62-65)
having an underside surface portion being fixed to
said peripheral surface portion of the bed (51-54)
surrounding said semiconductor chip (55-61)
without contact between said printed circuit board
(62-65) and said chip (55-61);

at least one opening being formed in each of the printed circuit boards (62)-65) for enclosing therein a respective semiconductor chip (55-61) in the or each opening;

connecting terminals of neighbouring printed circuit boards being connected by bonding wires (70); and

connecting terminals facing the leads (66) and the leads being connected via said TAB tapes (71)."

- VII. The appellant presented essentially the following arguments in support of his request:
- (a) The TAB tape 17 in document D5 does not fall under the term "printed circuit board", since the latter has a wiring pattern "printed" on a relatively stiff or rigid board. In contrast, a TAB tape is formed by sticking a thin-film wire on a resin film and therefore lacks the rigidity of a printed circuit board. It also follows from the normal usage of "board" and "tape" that a higher degree of stiffness is implied for a board than for a tape.
- (b) Thus, the subject matter of claim 1 differs from the device of document D5 in that (i) a printed circuit board is used instead of TAB tape, and (ii) the second connection means is a TAB tape instead of direct bonding.

(c) The technical problem addressed by the present invention is how to bridge a relatively large gap between the lead frame and the chip. In the device of document D5, the TAB tape would have insufficient rigidity for spanning large gaps.

The solution provided by the present invention is to use a printed circuit board to bridge the gap and to use a TAB tape connecting the printed circuit board to the lead frame. This construction provides added mechanical stability and, at the same time, a necessary degree of flexibility in the connection between the chip and the lead frame.

- (d) Document D5 does not provide any incentive to replace the TAB tape by a printed circuit board. Nor does any other prior art documents teach the use of a printed circuit board to bridge the gap between a semiconductor chip and a lead frame:

 Document D4 appears to disclose only a hybrid circuit formed in an integrated circuit package.

 Although document D2 discloses a bridging member, this is not a printed circuit board, but rather of a type similar to the TAB tape disclosed in document D5.
- (e) Even if the skilled person would have replaced the TAB tape in the device of document D5 with a printed circuit board, there is no incentive to use a TAB tape between the printed circuit board and the lead frame, in particular since it would be possible to use a device having the lead frame directly bonded to the printed circuit board. The use of a TAB tape, on the other hand, allows for an added degree of flexibility and an overall reduction of weight.

Reasons for the Decision

- 1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.
- Amendments and clarity

Since the wiring pattern on the surface of the printed circuit board (33) is on the same side as the first connecting means (37) with respect to the printed circuit board, claim 1 is identical in meaning to claim 1 according to the main request which was under consideration in the decision under appeal (cf. item II above). It is based on the embodiment of Figure 3 of the application as filed. Independent claim 4 is based on the embodiment of Figures 7 and 8 of the application as filed.

The Board also considers the claims on file to be clear and concise. It is in particular justified to have two independent claims in the light of the differences between the device of claim 1 where the printed circuit board 33 extends beyond the periphery of the bed 31, whereas in the embodiment of Figures 7 and 8, this is not necessarily the case.

- Inventive step Claim 1
- Document D5 discloses a chip package device comprising a chip 20 attached to a bed 13 and leads 11 of a lead frame, where the chip and lead frame are conventionally encapsulated in e.g. an epoxy or a plastic molding compound (cf. Figures 2 and 3; column 1, lines 23 to 27). The device of document D5 is designed for packaging a semiconductor chip with a high number of electrodes arranged on its surface. A relatively large distance between the electrodes on the chip surface and

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the leads of the lead frame results from the high density of connections, and an additional element is provided to bridge this gap between the lead frame and the chip and provide an interconnection from the chip to the lead frame (cf. column 3, lines 41 to 57). As a concrete example of such an additional element, a TAB tape 17 with conductive fingers 16 is positioned between the lead frame and the chip (cf. column 4, lines 14 to 33). The outer dimension of the TAB tape can be greater than the size of the bed 13 (cf. column 4, lines 5 to 9). The conductive fingers are bonded to the leads 11 of the lead frame on one side, and are connected to the chip 20 via bonding wires 22 (cf. column 5, lines 11 to 16 and 25 to 28).

- In the decision under appeal, it was held that the term "printed circuit board", as used in claim 1, would also include a TAB tape as known from document D5 (cf. item III(b) above).
- 3.2.1 The Board agrees however with the submissions made by the appellant that a person skilled in the art would not consider a TAB tape to fall under the term "printed circuit board", mainly because it is implicit that the insulating substrate of a printed circuit board has a higher degree of stiffness or rigidity than the polyimide film providing the backing of the TAB tape as known from document D5 (cf. item VII(a) above).

Furthermore, since claim 1 contains both the terms
"printed circuit board" and "TAB tape" in the context
that the TAB tape is connected to the second ends of
the printed circuit board, it is apparent that a
deliberate difference is made between a "TAB tape" and
"printed circuit board". A broad interpretation of

"printed circuit board" would on the other hand result
in a device having a TAB tape attached to yet another
TAB tape. Notwithstanding the question whether such an

interpretation would be considered as reading claim 1 with an attempt to make technical sense out of it (cf. Guidelines C-III, 4.2), a device having two TAB tapes attached to each other is neither disclosed nor suggested in any manner in the description.

- Thus, the subject matter of claim 1 according to the main request differs from the device of document D5 in that (i) a printed circuit board is used instead of TAB tape, and (ii) connection between the printed circuit board and the leads (second connection means) is in form of a TAB tape, whereas in document D5, direct bonding is used to connect the TAB tape to the lead frame.
- 3.4 According to the application as filed, the present invention relates to a device where a very small semiconductor chip having many in/out electrodes is connected to a lead frame. Due to the fact that the spacing between the leads of a lead frame cannot be made arbitrarily small, the distance between the lead frame and the semiconductor chip increases with the number of electrodes, and quickly becomes larger than what can reliably be bridged using conventional bonding wires (cf. the application as published, column 1, lines 17 to 34).
- 3.4.1 The device of document D5 as described above is also designed to solve the above problem of connecting a semiconductor chip having a large number of electrodes to a lead frame. As convincingly argued by the appellant, however, due to the use of a TAB tape in the device of document D5, the ability of the device of document D5 to solve this technical problem is limited: When a very large number of electrodes compared to the size of the semiconductor chip has to be connected, the

distance between the chip and the lead frame becomes so large that a TAB tape, due to its limited rigidity, is inadequate for providing a mechanically stable and thereby reliable connection (cf. item VII(c)).

- 3.4.2 Thus, having regard to the closest prior art, the objective technical problem addressed by the application in suit therefore relates to improve further the stability and reliability of the electrical connections between semiconductor chip and a lead frame when the size of the semiconductor chip becomes very small compared to the opening of the lead frame.
- The Board agrees with the submissions of the appellant that document D5 does not contain any incentive for replacing the TAB tape with e.g. a printed circuit board (cf. item VII(d) above). On the contrary, another embodiment of document D5 features a larger size bed 13 such that the entire TAB tape is supported by the bed (cf. D5, column 4, lines 5 to 8; Figure 2). Thus, as document D5 already contains a satisfactory solution to the above technical problem, there would be no reason for the skilled person to depart from the use of a TAB tape.
- 3.6 Also the other available prior art documents fail to suggest the use of a printed circuit board as an intermediate connection for bridging the gap between a semiconductor chip and a lead frame:
- 3.6.1 In document D2 (cf. Figure 2), conductive tracks 31 are formed on an insulating layer 30 of e.g. polyimide, where the entire insulating layer is formed on a bed 17 supporting a semiconductor chip 20. Thus, document D2 does not suggest the use of a printed circuit board.

- 3.6.2 Document D4 (cf. the abstract) shows a semiconductor chip 15 formed on a bed 8 and a printed circuit board 11 attached to the bed 8. Although the leads 9 of the lead frame are attached to the printed circuit board 11, it is only an insulating bonding 12 and the connection between the lead frame and the chip is through bonding wires 18. As evident from Figures 1 and 2, some bonding wires 18 are directly connected between the chip 15 and leads 9. Therefore, the circuit board does not function as an intermediate connection between the lead frame and the semiconductor chip, but is only used for interconnecting other components forming a hybrid circuit.
- Moreover, even assuming that the skilled person nevertheless has decided to replace the TAB tape of the device of document D5 with a printed circuit board, the Board agrees with the appellant that it would be difficult to conceive that the skilled person would then return to a TAB tape for the connection between a printed circuit board and a lead frame, in order to arrive at a device having the features (i) and (ii) (cf. items VII(e) and 3.3 above). This is in particular unlikely given the fact that the direct bonding technique, as taught in document D5, also appears to be suitable for connecting the lead frame to a printed circuit board.
 - 3.8 Therefore, in the Board's judgement, the subject matter of claim 1 involves an inventive step within the meaning of Article 56 EPC.

Since claims 2 and 3 are dependent on claim 1, the subject matter of these claims involves an inventive step as well.

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- 4. Inventive step Claim 4
- 4.1 It follows from the discussion under items 3.1 to 3.3. above that the subject matter of independent claim 4 differs from the device of document D5 not only in the features (i) printed circuit boards are used instead of TAB tape, and (ii) connection between the printed circuit board and the leads (second connection means) is form of a TAB tape, but also in that (iii) a plurality of semiconductor chips are mounted with a plurality of printed circuit boards, whereas document D5 only discloses a moulded material semiconductor device for sealing a single semiconductor chip.
- As already discussed under items 3.4 to 3.7 above, the Board is of the view that it is not obvious to modify the device of document D5 in such a manner to arrive at a device having the features (i) and (ii). In addition, none of the available prior art documents discloses a plurality of semiconductor chips distributed of a plurality of printed circuit boards in a moulded material device.

Therefore, in the Board's judgement, the subject matter of independent claim 4 involves an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided that:

- 1. The decision under appeal is set aside.
- 2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of:

Claims: 1 to

1 to 4, filed in the oral proceedings;

Description: pages 3a and 4, filed in the oral

proceedings,

pages 1 and 5 to 8, filed with letter

dated 3 January 1996,

page 2 as originally filed;

Drawings:

Figures 1 to 8 as originally filed.

The Registrar:

The Chairman:

D. Spigarelli

M. Chomentowski

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