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DECISION of 27 November 2001

0379170

Case Number:	т 0750/96 - 3.4.3
Application Number:	90100917.5

Publication Number:

IPC: H01L 23/522

Language of the proceedings: EN

Title of invention: Semiconductor device comprising wiring layers

Applicant:

KABUSHIKI KAISHA TOSHIBA

Opponent:

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Headword:

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Relevant legal provisions: EPC Art. 84

Keyword:

"Features in a claim defined by a result to be achieved" "Clarity (yes, after amendments)"

Decisions cited: T 0068/85

Catchword:

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Boards of Appeal

Chambres de recours

Case Number: T 0750/96 - 3.4.3

D E C I S I O N of the Technical Board of Appeal 3.4.3 of 27 November 2001

Appellant:	KABUSHIKI KAISHA TOSHIBA		
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	Kanagawa-ken 210-8572 (JP)		

Representative:	Lehn, Werner, DiplIng. Hoffmann Eitle	
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Decision under appeal:	Decision of the Examining Division of the
	European Patent Office posted 3 April 1996
	refusing European patent application
	No. 90 100 917 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman:	R.	к.	Shukla
Members:	Ε.	Wol	Lff
	М.	J.	Vogel



Summary of Facts and Submissions

I. This is an appeal from a decision of the Examining Division, dated 3 April 1996, to refuse European patent application No. 90 100 917.5 on the ground that the invention as claimed lacked novelty contrary to the requirements of Article 52(1)and Article 54(1), (2) EPC.

The decision of the Examining Division was based on the following document:

D2: Patent Abstracts of Japan, volume 10, No. 164 (E-410) [2220]; 16 May 1987; and JP-A-61-015 350.

A further document, US-A-4 695 868, was referred to in the decision as providing confirmation of the Examining Divisions arguments concerning the function of certain features (the slits) in document D2.

Also referred to but not relied upon in the decision were documents

- D1: Patent Abstracts of Japan, volume 11, No. 152 (E-507), 16 May 1987; and JP-A-61-288 439,
- D3: Patent Abstract of Japan, volume 12, No. 60 (E-584), 23 February 1988; and JP-A-62-202 525.

Claim 1 as refused by the examining division read as follows:

"1. A semiconductor device having a multilayered wiring structure, comprising:

(a) a substrate (5);

(b) a lower wiring layer (1) formed above the substrate (5);

(c) an insulating layer (6) formed on the lower wiring layer (1) and having a contact hole (3);

(d) an upper wiring layer (2) formed on the insulating layer (6) and connected to the lower wiring layer (1) through said contact hole (3);

(e) at least one slit (4a; 4a, 4b; 4a, 4b, 4c;4a, 4b, 4c, 4d; 4aa, 4bb, 4cc, 4dd) provided in said lower wiring layer (1); and

(f) said insulating layer (6) being formed in
the at least one slit (4a; 4a, 4b; 4a, 4b, 4c;
4a, 4b, 4c, 4d; 4aa, 4bb, 4cc, 4dd);

characterized in that

(g) said at least one slit (4a; 4a, 4b; 4a, 4b, 4c; 4a, 4b, 4c, 4d; 4aa, 4bb, 4cc, 4dd) is formed around the contact hole (3) to prevent movement of the lower wiring layer towards the contact hole (3)

The examining division concluded that this claim lacked novelty over document D2. Not only were all the features of paragraphs (a) to (f) shown in

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document D2, but the slits in document D2 were formed around the contact hole within the meaning of the wording of claim 1 and were filled with insulating material. Because any substantial movement of the lower wiring layer would inevitably cause cracks in the insulating layer, the function defined by feature (g) must be met in the known device. Therefore, the claim did not define any difference over the prior art.

The argument that the slits of document D2 are of considerable length and did not provide a "stopping face", was not accepted by the examining division. In the view of the examining division the application as filed provided no basis for these arguments. Citing document US-A-4 695 868 in support, the examining division concluded that irrespective of how inhibition of cracks was achieved, the arrangement of slits in document D2 definitely achieved the function specified in paragraph (g) of the claim.

Moreover, relying in particular on Figures 4 and 7 of the application, the examining division considered that the functional definition given by feature (g) of the claim did not lead to a clear and unambiguous definition of "stopping faces".

II. The notice of appeal was filed on 17 May 1996 and the appeal fee was paid on the same day. The statement setting out the grounds of appeal was filed on 8 August 1996, together with a new set of claims.

> In a written communication dated 6 July 2001, the Board informed the appellant that it did not consider that claim 1 filed with the statement of the grounds

of appeal satisfied the requirements of the EPC. In the preliminary view of the Board, the claim was not clear, contravened the provisions of Article 123(2) and lacked novelty having regard to document D2.

III. Oral proceedings took place on 27 November 2001.

IV. At the oral proceedings the appellant filed a new request which superseded all previous requests and which consisted of the following documents:

Claims: claims 1 to 7

Description: pages 1, 2, 2a, 3 to 9

Drawings: Figures 1 to 9.

Claim 1 of the request reads as follows:

"1. Semiconductor device comprising:

a substrate (5);

a lower wiring layer (1) formed above said substrate (5);

an insulating layer (6) formed on said lower wiring layer (1) having a contact hole (3);

an upper wiring layer (2) formed on the insulating layer (6) and being connected to said lower wiring layer (1) through said contact hole (3);

at least one slit (4a; 4a, 4b; 4a, 4b, 4c; 4a, 4b, 4c, 4d; 4aa, 4bb, 4cc, 4dd) formed in said lower wiring layer (1) in the vicinity of said contact hole and extending along one side of a contact region which is defined as a region which is located near the contact hole (3) and in contact with the upper wiring layer (2); and

an insulating portion (6a, 6a, 6b; 6a, 6b, 6c; 6a, 6b, 6c, 6d; 6aa, 6bb, 6cc, 6dd) formed integrally with the insulating layer (6) and being embedded in said slit (4a; 4a, 4b; 4a, 4b, 4c; 4a, 4b, 4c, 4d; 4aa, 4bb, 4cc, 4dd) whereby movement of the lower wiring layer within said contact region due to thermal expansion during annealing is prevented.

V. The arguments put forward by the appellant can be summarised as follows.

The invention concerns semiconductor devices, and addresses the problem of deformation in an upper wiring layer in the vicinity of a contact hole, caused by thermal expansion in a lower wiring layer as a result of annealing during the manufacture of the semiconductor device. The result of the expansion is upward projection of the upper wiring layer in the area around the contact hole, which, as explained in the application, can cause short circuits and the like. The present invention prevents these adverse effects of thermal expansion by forming in the vicinity of the contact hole a slit in the lower wiring layer which is filled with insulating material when the insulating layer is formed on top of the wiring layer. The mechanical connection between the insulating layers below and above the wiring layer act in the manner of a clamp which fixes the wiring layer in place and prevents movement of the wiring

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layer in the vicinity of the contact hole. This distinguishes the invention from the cited prior art which does not even address the same problem as the present invention. Document D2 in particular, which constitutes the nearest prior art, provides slits running longitudinally along the electrical conductors to divide this conductors into several smaller strips and so reduce the tendency of the insulating layer to form cracks.

Concerning the previously used term "around" to describe the location of the slits in relation to the contact hole, it is clear, in view of the number of embodiments shown in the application, that the term means "in the vicinity of the contact hole" as now claimed, rather than implying that the slits have to surround the contact hole.

Reasons for the Decision

- 1. The appeal is admissible.
- 2. Clarity (Article 84 EPC)
- 2.1 In claim 1 the location of one or more slits in relation to a contact region and the provision of the embedding insulating material in the slit(s) are defined by a result to be achieved ie "whereby movement of the lower wiring layer within said contact region due to thermal expansion during annealing is prevented". It is the established case law of the Boards of Appeal that functional features in terms of a result to be achieved are permissible in a claim if, from an objective view point, such

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features could not otherwise be defined more precisely without restricting the scope of the invention, if these features contain instructions which are sufficiently clear for the skilled person to reduce them to practice without undue burden and if the clarity of the claim is not jeopardised (T 68/85 (OJ EPO 1987, 228)). The application in suit contains examples of several different slit configurations with one or more slits. All the embodiments have in common that they aim to prevent the thermal expansion of the lower wiring layers during annealing from causing the upper wiring layer to project upwardly. The skilled person would have no difficulties in ascertaining whether or not a particular arrangement of the slits in the vicinity of a contact region prevented the upward projection of the upper wiring layer. The Board is also satisfied that the annealing conditions during manufacturing of a semiconductor device are well known in the art so that the condition under which the desired result is to be achieved are also clearly defined. The Board therefore accepts that it is appropriate to limit the claim in terms of functional features and that the claim is clear in this respect.

The Board is therefore satisfied that claim 1 is clear.

3. Amendments (Article 123 (2) EPC)

Claim 1 of the request differs in substance from claim 1 as originally filed in that its specifies

(i) the definition of the contact region;

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- (ii) that the slit is formed in the vicinity of the contact hole and extends along one side of the contact region;
- (iii) that the insulating portion is formed integrally with the insulating layer; and
- (iv) that within the contact region movement of the lower wiring layer due to thermal expansion during annealing is prevented.

The originally filed claim 1 specified that at least one slit is formed "around" the contact region. In response to a comment by the Board that the term "around" as used in the originally filed claim 1 and in claim 1 as rejected by the examining division lacked clarity, the appellant introduced the wording "in the vicinity of that contact hole and extending along one side of the contact region," and provided a definition of the term "contact region" within the claim. In the light of the variety of embodiments described to illustrate the invention, the new wording does not present the skilled person with any new information and therefore the amendment does not introduce any new subject-matter.

In the application as filed the term "contact region" had been defined in two different ways (page 4, lines 31 to 36). The definition of the term contact region introduced into claim 1 by amendment is identical with one of those definitions, and accords with the described embodiments.

Concerning the functional limitation to movement of the lower wiring layer "within the contact region due to thermal expansion during annealing," the basis for this restriction is to be found in the description of the application as filed (e.g. page 1 line 21 to page 2 line 1-which is part of the explanation of the problem addressed by the present invention, page 3 lines 7 to 11, and page 5 lines 21 to 26)."

That the insulating portions are "formed integrally with the insulating layer" is described for example in the description of Figure 2a and 2b on page 4, lines 27 to 29, and in connection with Figures 3 to 10 on page 6, lines 14 to 16.

The Board is therefore satisfied that none of these amendments introduces any subject-matter not contained in the application as originally filed.

4. Novelty (Articles 52(1) and 54 EPC).

The application had been rejected by the Examining Division as lacking novelty over document D2.

The claim now requires that at least one slit is formed in the lower wiring layer, and that it is formed in the vicinity of the contact hole and extending along one side of a contact region defined in the claim.

The slits disclosed in document D2 do not extend along one side of a contact region. Also, none of the other cited documents, D1, D3 and D4, disclose slits which exhibit all the features required by claim 1.

The invention as claimed is therefore novel.

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5. Inventive step (Articles 52(1) and 56 EPC)

Taking document D2 as having the closest structural similarities and therefore as presenting the closest prior art, the invention as claimed is distinguished from the device described in document D2 by the slit or slits formed in the lower wiring layer being formed in the vicinity of the contact hole and extending along one side of a contact region defined in the claim.

The invention in suit provides for a semiconductor device in which insulating material formed in a slit in a lower wiring layer prevents thermal expansion in the wiring layer from adversely affecting the device geometry in the vicinity of a contact hole. It is clear in particular from the description of the various embodiments that this effect is achieved by the lower wiring layer being anchored in position by the insulating material filling the slit formed in it.

Document D2 addresses the problem of cracks developing in an insulating layer covering a wiring layer, and it proposes to solve this problem by subdividing a conductor track into several parallel, narrower tracks separated by slits extending in the direction of the conducting track. As submitted by the appellant, document D2 thus teaches away from providing a slit extending along one side of the region surrounding the contact hole as in the claimed invention.

Document D1 aims to prevent cracking in an insulating layer provided between a lower wiring layer and an upper wiring layer at their crossover by means of one or more longitudinal slits in the lower wiring layer at the crossover, which divide the layer into narrower, parallel subsections. Thus, document D1 does not address the problem with which the application in suit is concerned, and does not teach to provide at least one slit which extends along one side of a contact region between the upper and lower wiring layers.

Document D3 provides for a slit in a guard ring which allows expansion to occur without generating cracks in a passivation film, and document D4 provides a conductor in the form of a grid pattern which prevents cracks forming in glass overlying the conductor.

Neither document D2 nor any of the other cited documents provide any measures for anchoring the wiring layer in place and there by prevent thermally induced movement of the wiring layer in the vicinity of the contact hole. Thus, neither the problem addressed nor the solution claimed are apparent from the contents of the prior art documents. The Board therefore concludes that the invention as claimed in claim 1 involves an inventive step.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first

instance with the order to grant a patent on the basis of the following documents, all filed during the oral proceedings.

Claims: 1 to 7,

Description: pages 1, 2, 2a, 3 to 9,

Figures: 1 to 9.

The Registrar:

The Chairman:

D. Spigarelli

R. Shukla