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D E C I S I O N
of 22 September 1999

Case Number: T 0788/96 - 3.4.3

Application Number: 88301637.0

Publication Number: 0281324

IPC: H01L 21/318

Language of the proceedings: EN

Title of invention:
Improved passivation for integrated circuit structures

Applicant:
Advanced Micro Devices, Inc.

Opponent:
-

Headword:
Passivation layer/ADVANCED MICRO DEVICES

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - yes"

Decisions cited:
-

Catchword:
-

Case Number: T 0788/96 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 22 September 1999

Appellant: Advanced Micro Devices, Inc.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 22 March 1996 refusing European patent application No. 88 301 637.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: G. L. Eliasson
A. C. G. Lindqvist

Summary of Facts and Submissions

I. European patent application No. 88 301 637.0 was refused in a decision of the examining division dated 22 March 1996. The ground for the refusal was that the subject matter of claim 1 according to all the requests lacked an inventive step with respect to the prior art documents

D3: IEEE, 23rd Annual Proceedings of the International Reliability Physics Symposium, 1985, pages 126-137; and

D6: Patent Abstracts of Japan, vol. 3, No. 119, [E-142], 6 October 1979 & JP-A-54 097 372.

II. The appellant (applicant) lodged an appeal on 22 May 1996, paying the appeal fee the same day, and filed a statement of the grounds of appeal on 30 July 1996. Further, the appellant submitted the following documents with the statement of grounds:

D6a: Translation of JP-A-54 097 372;

D3a: Declaration by Mr William P. Funsten, one of the co-authors of document D3; and

D8: IEEE Transactions on Electron Devices, vol. ED-25, No. 10, pages 1185-1193 (1978).

The appellant requested grant of a patent based on the following documents:

Claims: 1 to 10 filed with the letter of 19 January 1994 (the main request of the decision under appeal);

Description: pages 1 to 5 and 10 to 22 as originally filed;
pages 6, 8, and 9 filed with the letter of 23 October 1992; and
page 7 filed with the letter of 19 January 1994

Drawings: sheets 1/2 and 2/2 as originally filed.

III. With letter of 23 August 1996, the appellant submits a copy of the following document, in which document D8 was cited:

D9: D. V. Morgan and K. Board, "An Introduction to Semiconductor Microtechnology, Second Edition," pages 34 and 35.

IV. Claim 1 under consideration reads as follows:

"1. A process for producing an integrated circuit structure wherein a silicon nitride passivation layer resistant to penetration by moisture and ion contaminants is provided over an underlying metal layer, and wherein either (a) the level of compressive stress in the passivation layer is controlled and/or (b) an intermediate layer is formed between the metal layer and the passivation layer to relieve the underlying metal layer from stresses induced by the compressive stress in the passivation layer, characterised in that the surface of the metal layer is implanted with ions of a non-reactive element to change the grain structure of the surface, whereby the formation of voids in the metal layer, induced by said compressive stress in said passivation layer, is inhibited."

V. In the decision under appeal, the examining division reasoned essentially as follows:

1. Document D3 discloses a method of producing an integrated circuit structure having the features of the pre-characterizing part of claim 1. The method of claim 1 differs from that of document D3 in that claim 1 specifies an additional step of ion implanting the metal layer whereas document D3 does not disclose such a process step.

2. The technical problem to be solved by the present application is two-fold: (i) the inhibition of void formation in the metal layer, whilst (ii) providing a good coverage of the passivation layer so that the passivation layer provides protection against moisture and ion contamination. In the application as filed, it is stated that the steps (a) and (b) - which are both known from document D1 - are as such sufficient at least to inhibit void formation partially (cf. application as published, column 5, lines 2 to 9).

3. Document D6 teaches that cracking of an insulating layer deposited on an aluminum metallisation layer can be avoided when the edge profile of the metallisation layer is obtuse. Such an edge profile can be obtained by ion-implanting the aluminum metallisation layer prior to patterning.

4. As Figure 16 of document D3 shows an aluminum metallisation layer with obtuse angles, a skilled person wishing to follow the teaching of document D3 and having knowledge of document D6 would therefore immediately recognize the relevance of the teaching in the latter document to the formation of the structures shown in document D3. As the implantation parameters in document D6

correspond to those employed in the present application, a change in the grain structure of the metallisation will also take place when the process of document D6 is used.

VI. The appellant presented essentially the following arguments in support of his requests:

1. The problem the present application seeks to solve is the prevention of void formation in a metal layer covered by silicon nitride passivation, and not the protection against ion and moisture contamination, as was held in the decision under appeal, since at the priority date of the present application, silicon nitride was known to provide perfectly adequate passivation layers. Since document D6 does not address problem (i), the skilled person would have no reason to combine documents D3 and D6. The Declaration by Mr Funsten supports the above argument.

2. At the priority date of the application in suit, it was customary to use anisotropic etching for patterning Al wiring in the manufacture of an integrated circuit. Thus, the skilled person would not regard document D6 as relevant, since the document concerns the problem due to the **isotropic etching** of an aluminum layer. As evidence of this technological development, documents D8 and D9 are cited.

3. In document D3a, it was argued *inter alia* that Figure 16 of document D3 was used to illustrate the lines of tensile and compressive stress in a theoretical model and that the actual slope of the edge of the wiring layer was not a matter of concern to the conclusion made in document D3.

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Amendments*

Claim 1 is based on claims 1 and 2 as filed and additionally includes the subject matter disclosed in page 9, line 11 to page 10, line 11 and page 11, lines 16 to 25 of the application as filed. The subject matter of the dependent claims is based on the dependent claims as filed and on the description of the application as filed. The description has been amended for consistency with the amended claim 1 and to acknowledge the prior art documents.

The application as amended therefore complies with Article 123(2) EPC.

3. *Clarity*

The claims are considered by the Board to be clear and therefore meet the requirements of Article 84 EPC.

4. *Prior art and novelty*

4.1 Document D3, which the Board considers the closest prior art, investigates stress induced voids in aluminum wiring layers covered with a silicon nitride layer, i.e., the same problem as that addressed by the present application. It is reported in document D3 that the number of voids increase with the stress applied to the wiring layers by the overlaying passivation layer

(cf. D3, abstract; page 128 to 129; Figures 7 and 8). The experiments were carried out with an oxynitride/nitride structure where the stress was controlled by varying the relative thicknesses of the two layers.

4.1.1 Thus, all the features of the pre-characterizing part of claim 1 are known from document D3. The method of claim 1 therefore differs from that of document D3 in that the additional step of ion-implanting the metal layer with non-reactive ions prior to the step of depositing the passivation layer is carried out in order to change the grain structure of the surface of the metal layer, whereas in document D3 no such measure is disclosed.

4.2 Document D6 concerns the problem of avoiding cracks in an insulating layer covering an aluminum wiring layer which has been patterned using an isotropic etching method. When an isotropic etching step is used for patterning the wiring layer, the edges of the wiring layer are curved due to the under-etching of the metal below the mask (cf. D6, Figure 1). By implanting Ar ions in the aluminum layer before masking and isotropic etching of the wiring layer, the patterned wiring layer has obtuse edges which allows for the passivation to cover the wiring layer without cracks (cf. D6, Figure 2). The acceleration voltage (50 to 180 keV) and doses (10^{14} to 10^{15} cm^{-2}) during the ion-implantation are both similar to the values given in the present application (cf. original claims 4 and 5).

The material of the insulation layer on the wiring layer is not specified. However it is derivable from the English translation (see D6a, page 3, fifth paragraph), that the insulating layer acts as a passivation layer protecting the Al wiring layer from moisture and other corrosive substances.

4.2.1 Thus, the only feature that the process of document D6 has in common with the process of claim 1 is that ion-implantation of the metal layer is carried out with non-reactive ions before the insulating layer is deposited on the metal layer.

4.3 The subject matter of claim 1 is therefore new within the meaning of Article 54 EPC.

5. *Inventive step*

5.1 In view of the difference between the method of claim 1 and that of document D3 discussed under point 4.1.1 above, in the Board's view, the technical problem addressed by the present invention can be regarded as inhibiting the void formation in the metal layer covered by a silicon nitride layer providing the desired protection against moisture and ion contamination (cf. the application as published, column 3, lines 24 to 32).

5.2 In this connection, contrary to the view of the examining division in the decision under appeal, the Board agrees with the appellant that at the priority date of the application, silicon nitride was known in the prior art to have superior passivation properties in relation to silicon oxide or silicon oxynitride (cf. also the application, column 1, lines 16 to 44). The use of silicon nitride as material for the passivation layer therefore provided the desired degree of protection against moisture and ion contamination, as cracking of the silicon nitride passivation layer was not known to be a problem for the prior art devices.

5.3 A skilled person following the teaching of document D3 and faced with the technical problem stated under point 5.1 above would in the Board's view find no reason to use the teaching of document D6 which is solely concerned with avoiding the formation of cracks in the insulating layer covering the metal layer, and does not discuss the problem of the formation of voids in the metal layer due to the stress induced by the compressive stress in the passivation layer. Document D6 is also not concerned with formation of cracks specifically in a silicon nitride passivation layer, but only concerns the general case of an insulating layer covering the metal layer. The present invention, on the other hand, concerns specifically the use of silicon nitride as a passivation layer and the problem of void formation in the underlying metal layer, due to such a use. To a skilled person concerned with the problem of void formation in the metal layer, therefore, document D6 does not provide any incentive to carry out ion-implantation.

5.4 Claim 1 does not specify any etching for patterning the metal layer, and in particular, does not exclude the use of isotropic etching for patterning the metal layer. Nevertheless, as the present invention concerns a process for producing an integrated circuit where, at the priority date of the application in suit, relatively narrow line-widths of the order of 1 to 2 μm were customary, the Board finds the appellant's submissions plausible that in practice the isotropic etching could not be employed to produce the narrow line-width pattern, and consequently, document D6 cannot be regarded as relevant to the present invention.

5.5 For the foregoing reasons, the subject matter of claim 1 in the Board's judgement is not obvious having regard to the cited prior art, and accordingly involves an inventive step as required by Article 52(1) EPC.

Claims 2 to 10 are dependent on claim 1 and therefore also involve an inventive step.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance to grant a patent on the basis of the following documents:

Claims: 1 to 10 filed with the letter of 19 January 1994 (the main request considered in the decision in suit);

Description: pages 1 to 5 and 10 to 22 as originally filed;
pages 6, 8, and 9 filed with the letter of 23 October 1992; and
page 7 filed with the letter of 19 January 1994

Drawings: sheets 1/2 and 2/2 as originally filed.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla