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D E C I S I O N
of 17 October 2000

Case Number: T 0994/96 - 3.5.1

Application Number: 94200320.3

Publication Number: 0600853

IPC: H04N 1/18

Language of the proceedings: EN

Title of invention:

Apparatus for optically writing information

Applicant:

ROHM CO., LTD.

Opponent:

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Headword:

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Relevant legal provisions:

EPC Art. 56

Keyword:

"Inventive step (no)"

Decisions cited:

-

Catchword:

-



Case Number: T 0994/96 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 17 October 2000

Appellant: ROHM CO., LTD.
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Kyoto (JP)

Representative: Hoijtink, Reinoud
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 13 August 1996
refusing European patent application
No. 94 200 320.3 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: R. R. K. Zimmermann
P. H. Mühlens

Summary of Facts and Submissions

- I. The appeal concerns European patent application No. 94 200 320.3 (publication No. 0 600 853) claiming several priority dates from Japanese applications, the earliest filed on 21 June 1988.
- II. In a decision posted on 13 August 1996, the examining division refused the application for the reason that the subject-matter claimed did not meet the requirement of inventive step in view of prior art document D1 (EP-A-0 141 880, published 22 May 1985).
- III. Against the refusal of its application the appellant filed a notice of appeal on 9 October 1996, requesting grant of a patent on the basis of the claims on file; the appeal fee was paid the same day. The statement setting out the grounds of appeal was subsequently filed on 30 October 1996 and included an amended claim 1 which reads as follows:

"An apparatus for optically writing or reading information comprising a row of optical dot array chips (5, 5'), each of which includes a plurality of optical dot elements (L1-L64) constantly arranged in the direction of said row, and a control circuit (IC) connected to the optical dot elements (L1-L64); the control circuit (IC) for said each chip (5, 5') comprising: a plurality of drive transistors (TR1-TR64) for selectively driving the optical dot elements (L1-L64); and a gate voltage setting circuit (27) which applies an adjustable gate voltage (VG) to the respective drive transistors (TR1-TR64); said gate voltage setting circuit (27) comprising a plurality of resistors (Ra, Rb, R1-R7) selectable for adjusting the

gate voltage (VG); characterised in that said gate voltage setting circuit (27) comprises a first resistor portion (Ra, Rb) connected between a source voltage supplying terminal (VDD) and a gate voltage supplying terminal (VG), and a second resistor portion which includes a plurality of parallel resistors (R1-R7) having different resistivities, the parallel resistors (R1-R7) being connected commonly to the first resistor portion (Ra, Rb) on one hand and to separate grounding terminals (GS1-GS7) on the other hand, only selected one or ones of the parallel resistors (R1-R7) being made effective by grounding the corresponding one or ones of the grounding terminals (GS1-GS7) while the other one or ones of the parallel resistors (R1-R7) remain ineffective, whereby the voltage division between the first resistor portion (Ra, Rb) and the second resistor portion provides the adjustable gate voltage (VG)."

- IV. In public oral proceedings held before the Board on 17 October 2000, the matters in issue were discussed, whereby the appellant's representative expressed his willingness to amend claim 1 with regard to its two-part form to bring it into compliance with the requirements of Rule 29(1) EPC.

The decision on the appeal was announced on the basis of the following requests:

The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of claim 1 as filed with the grounds of appeal dated 30 October 1996.

- V. The arguments submitted by the appellant are summarized

as follows:

The difference between the invention and the closest prior art, the apparatus disclosed in document D1, resided in the drive transistors for selectively driving the optical dot elements and in the particular voltage divider comprising parallel- and serial-connected resistors for setting the gate voltage of the drive transistors. By choosing appropriate resistance values for the resistors a particularly fine adjustment of the divider within a basic range, and thus a fine adjustment of the gate voltage were achievable. Furthermore, the grounding terminals for selecting the individual resistors of the parallel-connected portion would considerably simplify the adjustment of the voltage divider, which was another important advantage over the prior art.

Reasons for the Decision

1. The appeal complies with the requirements of Articles 106 to 108 and Rules 1(1) and 64 EPC and is thus admissible.
2. The primary issue to be decided is whether the subject-matter of claim 1 meets the requirement of inventive step, i.e. in terms of Article 56 EPC whether, or not, having regard to the state of the art the alleged invention is obvious to the person skilled in the art.
 - 2.1 The examining division did not refer to any other prior art document than to document D1 so that this document appears to be an appropriate starting point for assessing inventive step.

Document D1 discloses a recording apparatus sharing the following features with the apparatus defined in present claim 1:

It comprises a row of optical dot array chips (exposure modules 23), each of which includes a plurality of optical dot elements (for example, LED row 25) constantly arranged in the direction of said row, and a control circuit (control chip 35) connected to the optical dot elements. The control circuit comprises a plurality of drivers (42) for selectively driving the optical dot elements and a circuit for setting the control signal provided by the control circuit to the optical dot elements and an adjustable resistor array (59).

2.2 The following features, therefore, distinguish the alleged invention from the apparatus of document D1:

- (A) the drivers are or include drive transistors for selectively driving the optical dot elements,
- (B) the circuit for setting the control signal is a gate voltage setting circuit which applies an adjustable gate voltage to the respective drive transistors and
- (C) which comprises a voltage divider (connected as defined in the second part of claim 1) having first and second resistor portions for providing the adjustable gate voltage at their connection point,
- (D) whereby the second resistor portion includes a

plurality of parallel-connected resistors of which only selected one or ones are made effective by grounding respective grounding terminals.

- 2.3 The terms "gate" and "source" do not have a clear meaning when reading claim 1 in isolation. However, figure 16 of the application, for example, shows that the drive transistors TR1-TR64 are actually FETs (field effect transistors). Said terms should thus be understood to refer to the gate and source terminals of field effect transistors.
- 2.4 The use of transistors, and in particular of field effect transistors, for driving optical elements is normal practice as well as the voltage-control of field effect transistors via the gate signal.

With regard to the further features distinguishing claim 1, document D1, page 12, first paragraph has to be taken into account according to which fabrication tolerances of drivers and LEDs between LED arrays result in deviations from their nominal performance. As solution to this problem, the document suggests to provide an adjustable control signal for determining the mean current produced by the driver into its corresponding LED.

Applying this teaching to a FET type of control circuit the skilled person would consider it an obvious solution to provide an equivalent control function for the current provided by the drive FETs to the corresponding optical elements, i.e. to provide an adjustable control of the gate voltage signal applied to the drive FETs. Since at least insulated-gate FETs draw almost no current, the skilled person would

consider a resistive voltage divider connected between ground and source voltage supply as the simplest solution for providing the required functionality.

For the purpose of setting the control signal, document D1 (loc.cit.) proposes a resistor array of serial-connected resistors, adjusted by short-circuiting one or more of the resistors. In view of this teaching and the fact that parallel-connections and serial-connections of resistors are well known to be electrically equivalent, the skilled person would consider it an obvious solution to provide adjustability of the voltage divider by using a similar array of parallel-connected resistors. Grounding resistors as claimed is the measure which directly corresponds to shortening resistors in the equivalent serial circuit for adjusting the voltage divider.

Therefore, all differences which distinguish the alleged invention develop as indicated above in a straightforward and obvious manner from the prior art of document D1 and do thus not involve an inventive step.

2.5 The appellant argued that the claimed parallel connection of resistors allowed for a finer adjustment of the voltage divider than the serial connection of resistors disclosed in document D1. The Board does not accept this argument since for manifest technical reasons essentially the same gradation of resistance values can be achieved in parallel- and in serial-connection by choosing appropriately graded resistance values.

3. Since the subject-matter of claim 1 does not meet the

requirement of inventive step the decision of the examining division must be confirmed; the appellant's requests can not be allowed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

M. Kiehl

P. K. J. van den Berg