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**D E C I S I O N**  
**of 9 May 2001**

**Case Number:** T 1056/96 - 3.4.3

**Application Number:** 90106205.9

**Publication Number:** 0390219

**IPC:** H01L 27/105

**Language of the proceedings:** EN

**Title of invention:**

Semiconductor device and method of manufacturing the same

**Applicant:**

KABUSHI KAISHA TOSHIBA

**Opponent:**

-

**Headword:**

-

**Relevant legal provisions:**

EPC Art. 123(2), 56

EPC R. 88

**Keyword:**

"Inventive step (no - main request), (yes - auxiliary request)"

"Correction of error under Rule 88 EPC (allowed)"

**Decisions cited:**

G 0003/89, G 0011/91, G 0002/95

**Catchword:**

-



Case Number: T 1056/96 - 3.4.3

**D E C I S I O N**  
**of the Technical Board of Appeal 3.4.3**  
**of 9 May 2001**

**Appellant:** KABUSHIKI KAISHA TOSHIBA  
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**Decision under appeal:** Decision of the Examining Division of the  
European Patent Office posted 1 August 1996  
refusing European patent application  
No. 90 106 205.9 pursuant to Article 97(1) EPC.

**Composition of the Board:**

**Chairman:** R. K. Shukla  
**Members:** M. Chomentowski  
M. J. Vogel

## Summary of Facts and Submissions

I. European patent application No. 90 106 205.9 (Publication No. 0 390 219) was refused by a decision of the examining division dated 1 August 1996 on the ground that its subject-matter lacked an inventive step having regard to the prior art documents

D1: GB-A-2 080 024 and

D2: US-A-4 637 128.

II. Independent claims 1 and 2 of the set of claims forming the basis for the decision read as follows:

"1. A semiconductor device including a plurality of logic elements and memory elements formed on the same semiconductor substrate (600) having a first conductivity type (p), comprising:

(a) a region where said logic elements are formed, including a first field inversion preventive layer (605a) having a first impurity concentration ( $3 \times 10^{13}$ ) and said first conductivity type (p) below a first field oxide film (606) for isolating said logic elements; and

(b) a region where said memory elements are formed, including a second field inversion preventive layer (605b) of said first conductivity type (p) and having a second impurity concentration ( $1.5 \times 10^{13}$ ) lower than said first impurity concentration ( $3 \times 10^{13}$ ) below a second field oxide film (606) having a width for isolating active regions (607) of said memory elements;

wherein

- (c) said second field inversion preventive layer (605b) comprises:
  - (c1) a first impurity part (605c) having a third impurity concentration ( $5 \times 10^{13}$ ) higher than said first impurity concentration ( $3 \times 10^{13}$ ) at a substantially central portion of the bottom surface of said second field oxide film (606);
  - (c2) said first impurity part (605c) having a first width sufficient for preventing current from flowing due to inversion under the second field oxide film (606); and
  - (c3) a second impurity part (605b) having said second impurity concentration ( $1.5 \times 10^{13}$ ) lower than said first impurity concentration ( $3 \times 10^{13}$ ) at a majority portion of the bottom surface of said second field oxide film (606),
  - (c4) said second impurity part (605b) having sufficient width from an active region (607) of the memory region to the second impurity part (605c) for preventing punch-through current; and
  - (c5) wherein said first impurity part (605c) does not adjoin active regions (607) of said memory elements; and
  - (c6) wherein said second impurity part (605b) adjoins active regions (607) of said memory elements."

"2. A method of manufacturing a semiconductor device including a logic element region and a memory element region formed on the same semiconductor substrate (600) having a first conductivity type (p), comprising the following steps:

- (a) forming (Figure 6A) an oxide film (602) and an oxidation resistive film (603) on a surface of said semiconductor substrate (600);
- (b) patterning and removing (Figure 6B) parts of said oxidation resistive film (603)
  - to expose a first portion of said oxide film (602) to be used for forming a first field oxide film (606) isolating logic elements in said logic element region; and
  - to expose a second portion of said oxide film (602) to be used for forming a second field oxide film (606) for isolating memory elements in said memory element region; and
- (c) coating (Figure 6B) a first resist film (604) on said exposed second portion of said oxide film (602) and said remaining parts of said oxidation resistive film (603a) on the memory element region only;
- (d) implanting (Figure 6B) impurity ions (B+) of said first conductivity type (p), by using said first resist film (604) in said memory element region and said remaining parts of said oxidation resistive film in said logic element region as masks, through said first portion of said oxide

film (602) into said semiconductor substrate (600, 601) for forming a first field inversion preventive layer (605a) having said first conductivity type (p) and a first impurity concentration ( $3 \times 10^{13}$ ) close to the surface of said semiconductor substrate (600, 601) at said first portion;

- (e) removing (Figure 6C) said first resist film (604) from said memory element region and forming a second resist film (604a) on said exposed first portion of said oxide film (602) and said remaining parts of said oxidation resistive film (603a) on the logic element side only;
- (f) implanting (Figure 6C) impurity ions (B+) of said first conductivity type (p), by using said second resist film (604a) in said logic element region and said remaining parts of said oxidation resistive film (603a) in said memory element region as masks, through said second portions of said oxide film (602) into said semiconductor substrate (600) for forming a second field inversion preventing layer (605b) having said first conductivity type (p) and a second impurity concentration ( $1.5 \times 10^{13}$ ) lower than said first impurity concentration close to the surface of said semiconductor substrate (600) at said second portions;
- (g) removing (Figure 6D) said second resist film (604a) from said logic element side and thereafter coating a third resist film (604b) on said field oxide film (602) at said first and second portions and said remaining parts of said oxidation

resistive film (603a) on said logic element and said memory element side and patterning said third resist film (604b) at said memory element side and removing said third resist film (604a) at a third portion positioned at a central portion of said second field inversion preventive layers (605b); and

- (h) implanting (Figure 6D) impurity ions (B+) of said first conductivity type (p), by using said third resist film (604a) in said logic element region and in said memory element side as masks, through said third portion into said semiconductor substrate (600, 602; 605b) for forming at said central portion a third region (605c) close to the surface of said semiconductor substrate (600, 602) having a third impurity concentration ( $5 \times 10^{13}$ ) higher than said first impurity concentration ( $3 \times 10^{13}$ );

whereby

- (i1) said third region (605c) is made to have a first width sufficient for preventing current from flowing due to inversion under said second field oxide film (606); and

- (i2) said second region (605b) is made to have sufficient width from an active region (607) of the memory region to said third region (605c) for preventing punch-through current."

III. The examining division reasoned essentially as follows:

*Inventive step - claim 1*

The semiconductor device known from document D1 (see Figure 4 and the corresponding text) includes a plurality of logic elements and memory elements formed on the same semiconductor substrate having a first conductivity type (p), and comprises:

- (a) a region (II) where said logic elements are formed, including a first field inversion preventive layer (20) having a first impurity concentration (p) and said first conductivity type (p) below a first field oxide film (14b) for isolating said logic elements; and
- (b1) a region (I) where said memory elements are formed, including a second field inversion preventive layer (18) of said first conductivity type (p) and having a second impurity concentration (p+) higher than said first impurity concentration below a second field oxide film (14a) having a width for isolating active regions of said memory elements.

The subject-matter of claim 1 differs from the above known device in that

- (i) the second field inversion preventive layer (18) (for the memory elements) has a second impurity part (605b) having a second impurity concentration lower than said first impurity concentration (feature "b") at the bottom surface of said second field oxide film (feature "c3") and adjoining the active region of the memory elements (feature "c6"), said second impurity part (605b) having sufficient width from an active region of the memory region to



the second impurity part for preventing punch-through current (feature "c4"); that

(ii) the first impurity part (605c) does not adjoin active regions of said memory elements (feature "c5"); and that

(iii) the second impurity part (605b) occupies a majority portion of the bottom surface of said second field oxide film (feature "c3").

From these differences, it can be seen that the invention solves the objective problem of providing isolation between memory elements through the use of a conventional field oxide film having a field inversion preventive layer while at the same time providing a pn junction between the field inversion preventive layer and the adjoining memory active region, which should have a withstand voltage capable of withstanding a high programming or writing voltage, even when the dimensions of the isolation regions are reduced.

Such a problem in the context of electrically programmable memory devices is already known from document D2 (see column 1, line 45 to column 2, line 27).

A memory device having an isolating field oxide film with a field inversion preventive layer underneath and having two impurity concentrations (62, 64) - one low impurity concentration at a portion adjoining the active region of the memory elements, and a high impurity concentration at a substantially central portion which does not adjoin the an active region of said memory elements - is described in document D2 as

providing the same advantages as in the application (see column 2, lines 52 to 61 and Figure 3; Figure 4H and associated text on column 4, line 12 to column 5, line 41).

The skilled person would furthermore understand from documents D1 and D2 the claimed relationship between the three different impurity concentrations of the field inversion preventive layers under discussion.

Since documents D1 and D2 both concern field oxide isolated memory elements, a skilled person would find no impediment in combining their teachings and therefore regard as a normal design option to include the above features (resulting in the distinguishing features (i) and (ii)) in the device of document D1 in order to solve the objective problem.

The memory device as claimed further requires that the second impurity part (605b) occupies a majority portion of the bottom surface of the second field oxide (distinguishing feature (iii)). This feature is for maintaining a desired breakdown voltage (which is determined by the width and impurity concentration of portion (605b)) even when the dimensions of the memory (including the field oxide regions) are reduced.

Taking the device shown in Figure 3 of documents D2 as a starting point, it can be seen that there are many important structural features; reducing the size of these features is a non-trivial but well studied task known as "scaling". Some features can be shrunk linearly with improvement in process resolution and minimum feature size; others are constrained by operating parameters such as programming voltage.

In the present case, the width of the low impurity concentration is constrained by the high impurity concentration of the adjacent source/drain region and the high electric field caused by the high programming voltage - since the function of the low impurity concentration region is to increase the breakdown voltage of the pn junction. Its width must therefore remain essentially as it is. On the other hand, the width of the high impurity concentration region, which functions to prevent an unwanted inversion layer forming under the field oxide film, its function is primarily determined by its impurity concentration.

Thus, it would be apparent to the skilled person that as the dimensions of the memory are reduced in order to increase memory density, the width of the high concentration region (605c) becomes smaller, whereas on the other hand the width of the low concentration region (605b) must remain to provide a high breakdown voltage pn junction and its size would inevitably become the majority portion of the bottom surface of the field oxide film.

Thus, starting from the above mentioned objective problem to be solved the skilled person would routinely arrive at the solution as claimed in claim 1 from the teaching of documents D1 and D2 without the use of inventive faculty.

*Claim 2 (method of manufacturing)*

The arguments given above are equally applicable to the method of claim 2 which merely claims a sequence of steps of applying resist films, selectively removing resist films, and implanting impurity ions in order to

form the doped regions (605a, 605b and 605c) of the device of claim 1. In particular, repeating the method steps of the method of document D1 to selectively implant second and third regions comes within the scope of customary practice followed by persons skilled in the art, specially as the advantages thus achieved can be readily contemplated in advance. This is especially the case in view of the acknowledgement in document D2 that an impurity diffusion step must be carried out twice in the construction of the low doped and the high doped region under the field oxide film.

Although the order of implanting steps in the claimed method differs from the method of Document D1 it would be clear to the skilled person that the order is only significant to the extent that a masking step can be avoided if it is appropriate to implant certain regions twice - as in the method of document D1 (see Figures 7b to 7d), the order being thus not significant.

IV. The applicant lodged an appeal against this decision on 1 October 1996 paying the appeal fee on the same day.

With the statement of grounds of appeal, filed on 28 November 1996, the appellant filed new, amended claims 1 and 2. Claim 1 has been amended to remove impurity concentration values which were specified between brackets in the wording of claim 1 which formed the basis of the decision under appeal.

Moreover, a new drawing sheet 5/7 containing amended Figures 6A to 6F was filed replacing the original sheet and it was contended that the amendments were admissible under Rule 88 EPC as correction of an obvious error.

- V. In a response dated 9 April 2001 to a communication from the Board, the appellant filed a new claim 2.
- VI. During the oral proceedings of 9 May 2001, the appellant filed a new set of claims and requested that the decision under appeal be set aside and a patent be granted on the basis of the following requests:

**Main request**

**Description:** Pages 1, 2 and 4 to 14 filed with letter dated 16 May 1994;  
Pages 3, 3a and 3b filed with letter dated 7 June 1996;

**Claims:** No. 1 filed with letter dated 28 November 1996 (statement of grounds of appeal);  
No. 2 filed with letter dated 9 April 2001;

**Drawings:** Sheets 1 to 4, 6 and 7, as filed, and Sheet 5 filed with letter dated 28 November 1996.

**Auxiliary request:**

**Claims:** Nos. 1 to 9 filed during the oral proceedings of 9 May 2001, and

the description and the drawings as for the main request.

Claim 1 of the auxiliary request specifies at the end

of feature (c5):

**"and extends deeper into said semiconductor substrate (600) than said second impurity part (605b)".**

In claim 2 of the auxiliary request, there is a step h1) identical with the step (h) of the method claim forming the basis of the decision under appeal with an additional step h2) having the wording:

"wherein in said step h1) said third central region (605c) is formed such that it extends deeper into the semiconductor substrate (600) than the remaining regions (605b) of said second field inversion preventive layer (605b),".

Additionally, in claim 2 of the auxiliary request, there are no numerical values of impurity concentration in brackets and, in step i2), "said second region (605b) is" is replaced by "said second regions (605b) are".

VII. The appellant submitted the following arguments in support of his requests:

*Main request*

Contrary to document D1, which concerns EPROM memory cells comprising logic elements on the same substrate, document D2 does not concern such devices with memory cells and logic elements on the same substrate. Thus, a combination of the teachings would not be obvious to the person skilled in the art of document D1.

Moreover, the distinguishing feature specifying that

the second, adjoining region with low impurity concentration of the field inversion preventive layer adjoining the memory cell is **at a majority portion** of the bottom surface of the field oxide film of the memory part (feature (c3) of claim 1) is not disclosed in any of the documents D1 and D2. The reasoning of the examining division concerning this distinguishing feature is based on hindsight, i.e. it is only when knowing already the invention that the skilled person could arrive in an obvious way at the invention, and this is not permissible.

Therefore, the device of claim 1 of the main request involves an inventive step.

*Correction of error - Rule 88 EPC*

Concerning the requested correction of error in the Figures 6A to 6F, the correction is justified because the error is obvious and the solution (with a substrate of the same conductivity type as the field preventive layers) is the only solution which makes sense technically when considering Figures 6A to 6F and the corresponding text in the application as filed.

*Auxiliary request*

Claim 1 of the auxiliary request specifies additionally in feature c5) that the first impurity part (605c), which does not adjoin active regions (607) of the memory elements, extends deeper into said semiconductor substrate than the second impurity part (605b). This feature is disclosed in none of the documents D1 or D2 and is thus a further distinguishing feature which is not directly derivable from the combination of the

teachings of the documents D1 and D2.

Thus, there is a combination of two distinguishing features which is not directly derivable from the prior art. Moreover, the further distinguishing feature, which undoubtedly contributes to prevent current from flowing due to inversion under the second field oxide film (606) (feature c3) of claim 1) because of the increased depth of the higher doped region of the first conductivity type, does not result from routine practice when scaling the semiconductor device of, for instance, Figure 3 of document D2.

Therefore, the device of claim 1 of the auxiliary request involves an inventive step.

The method of claim 2 comprises a sequence of method steps which differ from those disclosed in document D1. A combination with the teaching of document D2 is not obvious because said document concerns a method based on a totally different principle, with anisotropically etching and implanting in the inclined walls and in the horizontal bottom wall of the etched cavity, this resulting in a differential doping in accordance with said inclination. Moreover, since none of the documents renders obvious a structure including the two "remaining distinguishing features" mentioned with respect to claim 1, no method steps leading to the formation of said features can be considered as being obvious. Therefore, the method of claim 2 involves also an inventive step.

## **Reasons for the Decision**



1. The appeal is admissible.
2. *Main request*
  - 2.1 Inventive step
    - 2.1.1 Claim 1 of the appellant's main request is in substance the same as claim 1 forming the basis for the decision under appeal.
      - 2.1.1.1 The Board agrees with the finding in the decision under appeal, and this has not been disputed by the applicant either, that the following features of the semiconductor device according to claim 1 which are not disclosed in the closest prior art document D1, are known from document D2:

- (i) The second field inversion preventive layer (18) (for the memory elements) has a second impurity part (605b) having a second impurity concentration lower than said first impurity concentration (feature "b") at the bottom surface of said second field oxide film (feature "c3") and adjoining the active region of the memory elements (feature "c6"), said second impurity part (605b) having sufficient width from an active region of the memory region to the second impurity part for preventing punch-through current (feature "c4"); and
- (ii) The first impurity part (605c) does not adjoin active regions of said memory elements (feature "c5").

With regard to the prior art documents D1 and D2 the appellant has argued that, contrary to document D1, which concerns EPROM memory cells comprising logic elements on the same substrate, document D2 does not concern such devices with memory cells and logic elements on the same substrate, so that a combination of the teachings would not be obvious to the person skilled in the art of document D1.

However, this argument is not considered as being acceptable because, as mentioned in document D2 (see column 6, lines 51 to 56; see also column 6, lines 60 to 67), generally, an insulated gate field effect transistor acting as a peripheral circuit of the memory cell is included in an EPROM, this allowing the use of common fabrication steps.

Therefore, document D2 is related to the technical

field of document D1.

- 2.1.1.2 In document D2, however, the region (64) with low impurity concentration of the field inversion preventive layer (62, 64) adjoining the memory cell is not disclosed as being **at a majority portion** the bottom surface of the field oxide film of the memory part, as in feature (c3) of present claim 1. Thus, in view of this difference, even by combining the teaching of both documents D1 and D2 (see Figures 4A to 4H and the corresponding text), one does not arrive directly at the structure of present claim 1.

The appellant has argued that the reasoning of the examining division concerning this distinguishing feature is based on hindsight, i.e. that it is only when knowing already the invention that the skilled person could arrive in an obvious way at the invention, and this is not permissible.

However, this argument is not convincing for the reasons already set forth in the decision under appeal:

Taking into consideration the respective functions of the different parts of the doped region at the bottom surface of the second field oxide isolating memory elements shown in Figure 3 of document D2, on the one hand, and the task of reducing the dimensions of the device ("scaling") to be effected, on the other hand, routine practice of adjusting in particular the lateral dimensions of said different parts would result, on the basis of said considerations, inevitably in a device having a low impurity concentration region (64) underneath a majority

portion of the bottom surface of the field oxide.  
Thus, the process of modifying the structure shown in said document and mentioned in the mentioned reasoning is not based on hindsight.

Therefore, the subject-matter of claim 1 of the appellant's main request does not involve an inventive step in the sense of Article 56 EPC and, consequently, this main request is not allowable (Articles 56 and 97(1) EPC).

3. *Auxiliary request*

3.1 Correction of an error

The appellant has filed a new drawing sheet 5 showing Figures 6A to 6F with the conductivity type of the substrate being modified from n-type to p-type and presented this as the correction of an obvious error in view of the description as filed and published on column 6, lines 7 to 9.

Indeed, as in the corresponding passage of the application as filed (see page 12, lines 6 to 8) the passage referred to states that, in this embodiment, a p-type well (601) is formed only on the logic element side of a **p-type semiconductor substrate (600)**.

Thus, the skilled reader will realise that there is an inconsistency between the description, on the one hand, and the **Figures 6A to 6F**, which show **the substrate (600) being of n-type**, on the other hand, and he can correct the information in the application as filed either by changing the text of the

description (to read "n-type") or by changing the drawings of Sheet 5.

Pursuant to Rule 88 EPC, second sentence, the correction must be obvious in the sense that it is immediately evident that nothing else would have been intended than what is offered as the correction, and it is referred in this respect to the opinions/decisions of the Enlarged Board of Appeal G 3/89, G 11/91 and G 2/95.

During the oral proceedings, the technical significance of the conductivity type of the substrate was discussed and it was concluded that, since taking into account that an n-type substrate would make no technical sense in view of the insulated gate field effect memory devices shown in the drawing and described in the description, nothing else than what is offered as correction could have been intended.

Therefore, in the Board's judgment, the corrections to Figures 6A to 6F under Rule 88 EPC are admissible.

### 3.2 Admissibility of the amendments

Claims 1 and 2 are based on independent claims 2 (device) and 7 (method of manufacturing) of the application as filed, respectively. The further main amendments resulting in the independent claims of the appellant's auxiliary request and concerning the second impurity part (605b) on the memory side occupying a majority portion of the bottom surface of said second field oxide film (606) of the device and the highly doped central region under the same field

oxide on the memory side extending deeper into said the semiconductor substrate (600) than said second impurity part (605b), as well as the method steps resulting in said structural features, are shown in the Figures 6A to 6F of the application as filed.

Therefore, the Board is satisfied that the European patent application has not been amended in such a way that it contains subject-matter which extends beyond the content of the application as filed (Article 123(2) EPC).

The description now states that, whereas Figures 1A to 1F, 2A to 2F, 3A to 3F, 4 and 5 show process steps for manufacturing a semiconductor according to examples leading to this invention, Figures 6A to 6F show a sequence of steps of manufacturing a semiconductor device according to a preferred embodiment of this invention. Therefore, there is no ambiguity about the examples showing different sequences of steps of masking and implanting being used as alternatives to the method of Figures 6A to 6F. Moreover, the structural features and method features are used consistently in the device and method claims.

The amendments to the description are thus consistent with the subject-matter of claim 1 as amended, and do not contravene Article 123(2) EPC.

3.3 Inventive step

3.4.1 Claim 1

Claim 1 of the auxiliary request specifies that (a)

the second impurity part (605b) of the second field inversion preventive layer has a second impurity concentration lower than the first impurity concentration at a majority portion of the bottom surface of said second field oxide film (606) and adjoins active regions (607) of said memory elements.

Moreover, claim 1 of the auxiliary request specifies in feature (c5) that (b) the first impurity part (605c), which does not adjoin active regions (607) of the memory elements, extends deeper into said semiconductor substrate than the second impurity part (605b).

Document D1 shows in Figure 4 a field inversion preventive layer (18) consisting of only one part. Moreover, the device resulting from the process shown in Figures 10a to 10p of said same document D1, which has indeed two parts under the isolating field oxide (49a), has however the higher doped and also deeper extending region adjoining the active region of the memory element, and this is contrary to claim 1 of the auxiliary request.

In document D2 (see Figures 3 and 4H) the central part of the second field inversion preventive layer does not extend deeper into the semiconductor substrate than the part with lower impurity concentration which is at the bottom surface of said second field oxide film (606) and which adjoins active regions (607) of said memory elements.

Therefore, the feature (b) of claim 1 of the appellant's auxiliary request is not directly derivable from the combination of the teaching of

documents D1 and D2.

As convincingly argued by the appellant, the distinguishing features (a) and (b) are not derivable from documents D1 and D2, and this is even more the case for the combination of these distinguishing features. It also follows that the combination of features (a) and (b) contributes to the prevention of the formation of inversion channel, since although the lateral extent of the central highly doped region is reduced during the scaling, the increased depth of the region can compensate for this lateral reduction. In the Board's view, the combination of the features (a) and (b) goes beyond the routine considerations involved in the scaling down of the device of document D1, and cannot be regarded as obvious to the skilled person.

Therefore, having regard to the state of the art, the subject-matter of claim 1 of the appellant's auxiliary request is not obvious to a person skilled in the art and thus involves an inventive step in the sense of Article 56 EPC.

#### 3.4.2 Claim 2

The method of claim 2 comprises a sequence of, in particular, masking, implanting and oxidizing steps which are specific for forming a semiconductor device having features such as those recited in claim 1. The claimed method differs from the method of Document D1 which comprises different sequences of method steps and which moreover cannot lead to a device comprising in particular, on the memory side, under the isolating field oxide, a low doped majority part



adjoining the active region of the memory and a highly doped substantially central part extending deeper into the semiconductor substrate. Document D2, (see Figures 4A to 4H) discloses a method whereby cavities for the isolating field oxide are first anisotropically etched and then ions are implanted in the cavity, thus obtaining automatically, in one implantation step, impurity concentrations on the lateral, inclined walls of the cavity which are lower than the concentration in the central part of the cavity. As already set forth here above with respect to the device of claim 1, the implanted central part with higher impurity concentration is not shown as being deeper than the lateral parts with lower impurity concentration, and no indication in this sense is derivable from the rest of the document either.

Starting from document D1, which concerns the manufacturing of both memory and logic elements on the same semiconductor substrate, the combination with document D2 is already not obvious in view of the different principles of masking and doping in both documents. Moreover, the combination of these prior art documents does not lead in an obvious way to a method with steps resulting in a device comprising the features (a) and (b) mentioned above.

Therefore, the subject-matter of claim 2 of the present auxiliary request also involves an inventive step in the sense of Article 56 EPC.

3.4.3 Claims 1 and 2 are thus patentable in the sense of Article 52(1) EPC.

The further claims or the auxiliary request are dependent claims which concern particular embodiments of claims 1 or 2, and they are thus also patentable.

## Order

### For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the examining division with the order to grant a patent on the basis of the following patent application documents:

**Description:** Pages 1, 2 and 4 to 14 filed with letter dated 16 May 1994;  
Pages 3, 3a and 3b filed with letter dated 7 June 1996;

**Claims:** Nos. 1 to 9 (auxiliary request) filed during the oral proceedings of 9 May 2001;

**Drawings:** Sheets 1 to 4, 6 and 7, as filed; and Sheet 5 filed with letter dated 28 November 1996.

The Registrar:

The Chairman:

L. Martinuzzi

R. K. Shukla