BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS | BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE | CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [X] To Chairmen

D E C I S I O N
of 27 October 1998

Case Number: T 0147/97 - 3.5.2

Application Number: 92911860.2

Publication Number: 0583371

IPC: H03K 19/177

Language of the proceedings: EN

Title of invention:
Output logic macrocell with enhanced functional capabilities

Applicant:
Lattice Semiconductor Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - yes"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0147/97 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 27 October 1998

Appellant: Lattice Semiconductor Corporation
5555 N.E. Moore Court
Hillsboro, Oregon 97124-6421 (US)

Representative: Fieret, Johannes, Ir.
Algemeen Octrooibureau
World Trade Center
P.O. Box 645
5600 AP Eindhoven (NL)

Decision under appeal: Decision of the Examining Division of the European Patent Office posted 24 September 1996 refusing European patent application No. 92 911 860.2 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: W. J. L. Wheeler
Members: R. G. O'Connell
A. C. G. Lindqvist

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 92 911 860.2 on the ground that the subject-matter of claim 1 filed with the letter dated 25 June 1996 did not involve an inventive step having regard to the following documents:

D1: US-A-4 789 951 and
D2: US-A-4 758 746.

II. The application as presently amended consists of the following documents:

Description: pages 1 to 4 and 7 to 11 as published in WO 92/20155, and pages 5, 6, 12 and 13 as filed with the letter dated 25 June 1996;

Claims: 1 to 25 as filed with the letter dated 25 June 1996;

Drawings: sheets 1 to 6 as published.

III. Claim 1 is worded as follows:

"An output logic macrocell for use with a logic circuit having a plurality of outputs, said macrocell comprising an exclusive OR gate having first and second inputs, said first input being connected to an output of a first OR gate having a plurality of inputs connected to outputs of said logic circuit, and further comprising means for switching said second input of said exclusive OR gate alternatively to an output of said logic circuit or to ground or to an output of a second OR gate having a plurality of inputs connected to outputs of said logic circuit."

Claims 2 to 25 are dependent on claim 1.

IV. The appellant argued in effect that D1 did not show "a second OR gate having a plurality of inputs connected to outputs of said logic circuit". The examining division had plucked this feature out of D2 (which showed two OR gates **permanently** connected to the inputs of an XOR gate) and inserted it into the structure shown in Figure 3 of D1, stating that it would be obvious to include "means for switching" as recited in claim 1. This was untenable, since there was no indication in either D1 or D2 that any useful purpose would be served by such a combination.

V. The appellant requested that the decision under appeal be set aside (main request). The appellant also filed an auxiliary request (claims 1 to 28 filed with the statement of grounds of appeal).

Reasons for the Decision

1. The appeal is admissible.

2. The main issue to be decided in this appeal is whether the output logic macrocell according to claim 1 involves an inventive step, having regard to the prior art known from D1 and D2.

3. D1 discloses an output logic macrocell for use with a logic circuit having a plurality of outputs, said macrocell comprising an exclusive OR gate (80) having first and second inputs, said first input being connected to an output of a first OR gate (70) having a plurality of inputs (68) connected to outputs (P1 to P8) of said logic circuit. The second input of said exclusive OR gate is permanently connected to an output

(79) of said logic circuit (see column 3, lines 54 to 59). A low output signal can be forced on the output (79) by leaving intact the fuses (64) between the input to AND gate (78) and both of the pair of complementary lines (63) from any of the phase splitters (62) connected to the inputs of said logic circuit (see column 4, lines 20 to 24).

4. It is apparent that once a fuse (64) has been blown in the D1 circuit it cannot be reinstated.

5. The output logic macrocell according to claim 1 differs from the prior art circuit disclosed in D1 in that it further comprises means for switching said second input of said exclusive OR gate alternatively to an output of said logic circuit or to ground or to an output of a second OR gate having a plurality of inputs connected to outputs of said logic circuit.

6. D2 discloses an output logic macrocell for use with a logic circuit having a plurality of outputs, said macrocell comprising an exclusive OR gate (see for example figure 4e, block 108-4) having first and second inputs, said first input being permanently connected to an output of a first OR gate having a plurality of inputs connected to outputs of said logic circuit, said second input of said exclusive OR gate being permanently connected to an output of a second OR gate having a plurality of inputs connected to outputs of said logic circuit.

7. The output logic macrocell according to claim 1 differs from the prior art circuit disclosed in D2 in that it further comprises means for switching said second input of said exclusive OR gate alternatively to an output of said logic circuit or to ground or to an output of said second OR gate.

8. Even if for the sake of argument it is assumed that it is obvious to a skilled person to modify the output logic macrocell known from D1 by connecting said second input of said exclusive OR gate to an output of a second OR gate having a plurality of inputs connected to outputs of said logic circuit in the manner known from D2, the result would not be an output logic macrocell according to claim 1, because there would be no means for switching said second input of said exclusive OR gate alternatively to an output of said logic circuit or to ground or to an output of a second OR gate having a plurality of inputs connected to outputs of said logic circuit.

9. In the judgement of the Board, the fact that it was known from D1 to provide options which could be exercised during programming by blowing fuses to leave the second input of the XOR gate connected to an output of the logic circuit or to force a low input signal on the second input of the XOR gate, and known from D2 to permanently connect the second input of the XOR gate to an output of a second OR gate having a plurality of inputs connected to outputs of said logic circuit, does not render it obvious to provide means for switching between the three options specified in claim 1 during the subsequent operational life of the circuit.

10. The board concludes therefore that the subject-matter of claim 1 involves an inventive step within the meaning of Article 56 EPC, having regard to the prior art according to D1 and D2.

11. The board has satisfied itself that as far as claim 1 is concerned the application has not been amended in such a way that it contains subject-matter which extends beyond the content of the application as filed.

12. The board has not examined claims 2 to 25 (other than to check that they are dependent on claim 1). Nor has the Board examined the description (apart from reading it to obtain an understanding of the invention). Rather than do this itself, the board makes use of its powers under Article 111(1) EPC to remit the case to the department of first instance for further examination. For avoidance of doubt, it is pointed out that according to Article 111(2) EPC the department of first instance is bound by the present decision only to the extent that the matters mentioned in paragraphs 10 and 11 above have been decided.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution.

The Registrar: The Chairman:

M. Kiehl W. J. L. Wheeler