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DECISION of 2 October 2001

Case Number:	Т 0366/97 - 3.4.3
Application Number:	90901362.5
Publication Number:	0449951
IPC:	H01L 29/24

Language of the proceedings: EN

Title of invention:

Ultra-fast high temperature rectifying diode formed in silicon carbide

Patentee:

CREE RESEARCH, INC.

Opponent: Siemens AG

Headword:

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Relevant legal provisions: EPC Art. 56

Keyword:

"Inventive step (affirmed)" "Closest prior art"

Decisions cited: T 0254/86, T 0656/90, T 0282/90, T 0989/93

Catchword:



Europäisches Patentamt European Patent Office Office européen des brevets

Beschwerdekammern

Boards of Appeal

Chambres de recours

Case Number: T 0366/97 - 3.4.3

D E C I S I O N of the Technical Board of Appeal 3.4.3 of 2 October 2001

Appellant:	Siemens AG	
(Opponent)	Postfach 22 16 34	
	D-80506 München	(DE)

Representative:

Respondent:				CREE	RE	SEARCH	INC.		
(Proprietor	of	the	patent)	2810	Me	ridian	Parkway,	Suite	176
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Decision under appeal:	Decision of the Opposition Division of the
	European Patent Office posted 28 February 1997
	rejecting the opposition filed against European
	patent No. 0 449 951 pursuant to Article 102(2)
	EPC.

Composition of the Board:

Chairman:	R.	К.	Shukla	
Members:	v.	L.	P.	Frank
	Μ.	J.	Vogel	

Summary of Facts and Submissions

I. The appellant (opponent) lodged an appeal on 20 March 1997 against the decision of the opposition division, dispatched on 28 February 1997, rejecting the opposition against the European patent No. 0 449 951. The fee for the appeal was paid on 20 March 1997. The statement setting out the grounds of appeal was received on 27 June 1997.

> The opposition was filed against the patent as a whole and based on Article 100(a) together with Articles 52(1) and 56 EPC.

The opposition division held that the grounds for opposition did not prejudice the maintenance of the patent as unamended, having regard *inter alia* to the following prior art documents:

- D1: Journal of Applied Physics, vol. 48, no. 11, November 1977, pp. 4831-4833
- D2: Soviet Physics Semiconductors, vol. 22, no. 2, February 1988, pp. 181-183.

During the opposition proceedings the following documents were cited by the opponent outside the opposition period (Article 99(1) and Rule 55(c) EPC):

- D7: "Semiconductor Devices" by S. M. Sze, John Wiley & Sons, 1985, pp. 103-107
- D8: Japanese Journal of Applied Physics, Vol. 2, No. 11, Nov. 1987, pp. L1815-L1817

- D9: Sov. Tech. Phys. Lett., Vol. 13, No. 10, Nov. 1987, pp. 523-524
- D10: "Werkstoffe der Halbleitertechnik" by H-F. Hadamovsky, VEB Deutscher Verlag für Grundstoffindustrie, 1985, pp. 113-114
- D11: "Silicon Carbide as a semiconductor" by
 J. Feitknecht, Springer Tracts in Modern Physics,
 58, 4, 1971, pp. 104-107.
- II. With the statements of grounds of appeal, the appellant cited the following documents:
 - D12: Technical Documentary Report No. AL TDR 64-253, Air Force Avionics Laboratory, Research and Technology Division, Air Force Command, Wright-Patterson Air Force Base, Ohio, pp. 98 and 111-113
 - D13: "Semiconductor Devices" by S. M. Sze, John Wiley & Sons, 1985, pp. 76-79 and 102-107
 - D14: DE-OS-1 956 011
 - D15: DE-OS-2 029 369
 - D16: US-A-3 986 193

D17: DE-OS-2 345 198

III. Prior to the oral proceedings, which were requested by both parties as an auxiliary request, the appellant informed the Board that he would not be represented at the oral proceedings and that his request for oral proceedings was thereby withdrawn.

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IV. The appellant requested

- that documents D7 to D11, which were disregarded by the opposition division under the provisions of Article 114(2) EPC, as well as documents D12 to D17 presented with the statement of grounds, be introduced into the proceedings, and

- that the decision under appeal be set aside and the patent be revoked in its entirety.

V. The respondent (patentee) requested

- that documents D7 to D17 be disregarded as late filed evidence under Article 114(2) EPC, and

- that the appeal be dismissed.

VI. The wording of independent claim 1 reads as follows and has been subdivided into paragraphs (a) to (h) by the Board for facilitating its discussion:

"1. A fast recovery, high temperature rectifying diode formed in silicon carbide and comprising:

a) a monocrystalline silicon carbide substrate
 having n-type conductivity;

b) an ohmic contact to said substrate;

c) a first monocrystalline epitaxial layer of ntype silicon carbide upon said substrate; and

d) a second monocrystalline epitaxial layer of silicon carbide upon said first epitaxial layer;

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characterized in that:

e) said second epitaxial layer has p-type conductivity and

f) a carrier concentration at least an order of magnitude less than the carrier concentration of said first epitaxial layer so that said second layer is predominantly depleted in reverse bias with said carrier concentration of said second layer being between about 1×10^{15} and 1×10^{18} atoms per cubic centimeter (cm⁻³), and

g) said second layer further having a minimum thickness of about 0.2 micrometers at a carrier concentration of about 1 x 10^{18} cm⁻³ and that may be increased proportionally to a thickness of about 70 micrometers at a carrier concentration of about 1 x 10^{15} cm⁻³ so that said minimum thickness is sufficient to achieve avalanche breakdown under reverse bias; and

h) an abrupt p-n junction formed between said first and second epitaxial layers such that the relationship between the reciprocal capacitance squared and the applied voltage is a substantially linear relationship."

VII. The appellant argued essentially as follows:

- Document D1 should be considered as the closest prior art, since it discloses a rectifying diode with the same pn⁺ abrupt junction as the one claimed in the patent in suit and since it is the junction which essentially defines the characteristics of a rectifying diode (see the patent in suit column 4, lines 36 to

39). The diode disclosed in document D2 on the other hand comprises a np^+ junction.

- Although the breakdown voltage of the device disclosed in document D2 is higher (300 V) than the one disclosed in document D1 (140 V), this fact cannot be interpreted as being due to the different layer structure of these diodes, since the breakdown voltage is mainly due to the crystal quality, the ratio of carrier concentrations and the doping level of the low doped side of the junction. A skilled person would consider that the higher breakdown voltage achieved in document D2 is due to the higher crystal quality of the epitaxial layers, since the last two properties mentioned previously are similar in both devices and since the fabrication of the device of document D2 benefits from the technological progress of nearly ten years. There are therefore no reasons for a skilled person to dismiss the disclosure of document D1.

- It is well known to the skilled person that a n-type substrate is preferable to a p-type one, since electrons have a much higher mobility than holes and, consequently, a n-type substrate with a similar carrier concentration than a p-type one has a much smaller resistance. This fact directly influences the forward resistance of the diode. A skilled person concerned with reducing the forward resistance would replace the p-type substrate used in document D1 by a substrate with the opposed polarity and thereby would arrive at the $n_{subst}/n^{*}/p$ structure as claimed.

VIII. The respondent argued essentially as follows:

- The whole structure of document D2 is closer to the

invention than the one of D1 and, in consequence, document D2 should be regarded as the closest prior art. For assessing the closest prior art mainly the properties exhibited by each structure have to be considered. A skilled person would consider the device of D2, with its improved properties, a much more promising starting point than D1. Furthermore, as specifically mentioned in document D2, the improvements achieved in breakdown voltage are due to the special layer sequencing and doping used.

- To arrive at the device of the present invention by starting from the device disclosed in document D1, the skilled person would have to replace the order of all the layers and would also have to change the conductivity type of the substrate. The analysis presented by the appellant is clearly based on hindsight, as the skilled person starting from D1 would promptly have to disregard all the teaching of this document, save for retaining the use of a pn⁺ junction as the sole feature of value to him.

- The statement that the substrate makes the greatest contribution to the diode's forward resistance is also contested by the respondent, as the influence of the larger substrate's thickness can be easily compensated by higher doping. There is no compelling reason to use a n-type substrate and p-type substrates are still employed for making rectifying SiC diodes.

- Furthermore, in the device according to the invention, it is the layer not in contact with the substrate which is depleted under reverse bias conditions. This is exactly the opposite structure to the one disclosed in documents D1 and D2 in which the

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blocking layer is adjacent to the substrate.

Reasons for the Decision

1. The appeal is admissible.

- 2. Late filed documents
- 2.1 The appellant has requested that documents D7 to D17 be introduced into the proceedings, since these documents illustrate the general background knowledge of the skilled person in the art.
- 2.2 The Board after having studied these documents has come to the conclusion that they are not relevant for the present decision and decides, under the provisions of Article 114(2) EPC, that documents D7 to D10 and D12 to D17 are not introduced into the proceedings, for the following reasons:

Documents D7 and D13 are extracts from a standard textbook on the physics of semiconductor devices. The general concepts exposed in these documents were, however, not contested by the respondent.

No arguments of the appellant are based on documents D8 to D10.

Document D12 supports the finding, already acknowledged in the patent in suit, that the properties of a rectifying diode are mainly defined by the properties of the pn junction used.

Document D14 is referred to by the appellant to show

that all possible combinations of substrate types and layer sequences at the pn junction were available to the skilled person.

Documents D15 to D17 disclose that n-type substrates were employed for manufacturing SiC rectifiers. This is, however, already disclosed in document D2.

- 2.3 Nevertheless, document D11 is admitted into the proceedings by the Board, as it discloses general background knowledge on silicon carbide (SiC) which is relevant to the consideration of inventive step.
- 3. Inventive step (Article 56 EPC)

The only remaining issue in the present appeal is that of inventive step.

3.1 Closest prior art

There is no agreement between the parties as to which of the documents D1 and D2 represents the closest prior art. The appellant has contended that document D1 is the closest prior art, since it discloses the same pn⁺ abrupt junction as the invention, which determines the characteristics of a rectifying diode. According to the respondent on the other hand, the device of document D2 having an overall device structure and properties similar to the structure and properties of the invention, respectively, is the closest prior art.

According to the established case law of the Boards of Appeal, an objective and realistic consideration of inventive step requires that certain criteria are followed in selecting the closest prior art. The first

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or the foremost consideration is that the closest prior art relates to the same or a closely related technical field as the invention (cf. T 989/93). Also, where several prior art documents meet this criterion, according to the case law, the closest prior art is the most promising starting point for demonstrating the obviousness of the invention having regard to the primary object of the invention (cf. T 254/86, OJ EPO 1989, 115; T 656/90 and T 282/90).

- 3.2 Consequently, in the following, document D1 will be considered as the closest prior art to assess inventive step of the subject-matter of claim 1.
- 3.2.1 Document D1 discloses a SiC diode formed of a p⁺-type substrate onto which a first epitaxial layer of p-type conductivity and a second epitaxial layer of n⁺-type conductivity are grown in this order. The junction formed by the p- and n-type layers is an abrupt one, as evidenced by the linear relationship between the reciprocal capacitance squared $(1/C^2)$ and the reverse voltage. The doping of the p-type layer is in the range of 10^{16} to 2 x 10^{18} cm⁻³ and the doping of the n⁺-type layer is at least one order of magnitude higher. The less doped p-type layer, which is in contact with the substrate, acts under reverse bias conditions as the blocking layer. Ohmic contacts are provided on the substrate and on the n^+ -type layer (cf. D1, Abstract; page 4831, left-hand column, last full paragraph; Figs. 1 and 3).
- 3.2.2 The pn⁺ abrupt junction disclosed in document D1, however, achieves a maximum breakdown voltage of about 150 V. The breakdown voltage of abrupt asymmetric junctions is, in a first approximation, inversely

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proportional to the carrier concentration of the blocking layer. This implies a linear relationship with a negative slope between these magnitudes in a double logarithmic representation (see Figure 19 of document D11). As is, however, shown in Figure 4 of document D1, the breakdown voltage curve stops increasing at a carrier concentration of about 10¹⁷ cm⁻³ and levels off at this value instead of following the predicted linear relationship for lower carrier concentrations. This is due, as explained in this document, to the mesa-etching technique employed which gives rise to an enhanced electric field at the periphery. The breakdown behaviour at lower doping levels is, therefore, dominated by edge effects and local crystal

imperfections and not by the junction itself (cf. page 4832, left-hand column, last but one paragraph).

- 3.2.3 The rectifying diode according to claim 1 of the patent in suit differs from this known rectifying diode essentially in that
 - (i) the conductivity type of the substrate and of the first and second epitaxial layers is of the opposite conductivity type (features (a), (c) and (e) of claim 1, see point V. above),
 - (ii) the carrier concentration of the second epitaxial layer is lower than the one of the first epitaxial layer (feature (f)), and in that
 - (iii) the minimum thickness of the second epitaxial layer is specified in dependence of the carrier concentration of this layer (feature (g)).

3.2.4 According to the patent in suit, it is an object of the

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invention to provide a SiC rectifying diode which operates at high frequency, high reverse voltage and high temperatures, having low forward resistance (cf. column 5, lines 29 to 33 of the published patent). The rectifier described in the specific embodiment shown in Figure 3 of the patent in suit achieves a voltage breakdown of about 400 V which is considerably higher than the breakdown voltage of 150 V obtained with the diode structure described in document D1. Also the diode of the invention is employed at a temperature of about 350°C and is suitable for high frequency applications, since it has a reverse recovery time of about 6 ns (cf. Figs. 11, 12, 14 and 15).

In consequence, the SiC rectifying diode as claimed solves the primary problem addressed in the patent in suit, taking document D1 as the closest state of the art.

3.2.5 The appellant has argued that the skilled person would consider the replacement of the p-type substrate used in document D1 by a n-type substrate as an obvious alternative, since n-type substrates have lower resistance than p-type substrates with the same doping level due to the higher mobility of the electrons and the low donor's ionization energy (cf. D11, page 106, lines 5 to 16). In order to avoid a further junction between the n-type substrate and the p-type blocking layer, he would position the substrate on the opposite side of the junction, i.e. in contact with the n⁺-type layer, obtaining a diode with the same structure as the one of the claimed invention.

The Board, however, is not convinced by the above argumentation, since it ignores the primary object of

the invention, i.e. an increase in the reverse breakdown voltage of the SiC diode, and additionally discards the overall arrangement of the semiconductor substrate and the semiconductor layers as well as the conductivity type of the substrate taught in the alleged closest prior art document D1. The appellant's argumentation, in the Board's view, is thus based on hindsight and cannot therefore be accepted.

- 3.2.6 Moreover, following the teaching of document D1, the skilled person, would try to reduce the crystal imperfections at the periphery and improve the edge properties of the mesa device with a view to enhance the reverse breakdown voltage. There is no suggestion in document D1 or any other prior art document reflecting the common general knowledge in the art that a change in the conductivity type of the substrate, with the resulting modification of the layering sequence, would improve the breakdown behaviour. This, however, is not contended by the appellant either.
- 3.2.7 The Board also cannot follow the argument of the appellant that the skilled person would preferably use a n-type substrate instead of the p-type substrate employed in document D1 in order to reduce the forward resistance of the rectifier, since it is the thickness of the low doped blocking layer which mainly determines the forward resistance, i.e. it is this layer which has the highest resistance (cf. D11, page 106, 2nd sentence). Furthermore, the difference in resistance between n- and p-type substrates is reduced at higher doping levels and, in consequence, both substrate types are, in principle, equivalent (cf. D11, page 106, lines 16 to 18). The contribution of the blocking layer to the total resistance of the diode is,

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however, not modified by a change in the conductivity type of the substrate.

- 3.2.8 For the foregoing reasons, in the Board's judgment, document D1 does not represent the closest prior art.
- 3.2.9 Consequently, it follows that the appellant's submissions regarding lack of inventive step based on document D1 as the closest prior art are not well founded and are not convincing.
- 3.3 Moreover, in the Board's view, the invention as claimed involves an inventive step even if , as submitted by the respondent, document D2 was regarded as the closest prior art, for the following reasons:
- 3.3.1 Document D2 discloses an abrupt junction SiC diode for high temperatures and high frequency (cf. D2, Abstract and page 182, rightmost column, 2nd full paragraph). This diode is formed by a n^+ -type substrate, a first epitaxial layer of n-type conductivity and a second epitaxial layer of p^+ -type conductivity. The impurity concentration of the n-type layer is in the range of 5×10^{16} to 10^{17} cm⁻³ and, under reverse bias conditions, it is this layer which will act as the blocking layer. Although the breakdown voltage achieved is in excess of 300 V, it is limited by leakage currents along the periphery of the mesa structure (cf. page 181, 2nd and 3rd paragraphs; page 182, 1st and 3rd paragraphs). The minimum effective lifetime of the minority carriers is estimated in this document to be of the order of 10 ns (cf. page 182, rightmost column, 2nd full paragraph). Such a short minority carrier lifetime is required for high frequency applications, as it allows fast switching polarization.

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- 3.3.2 The rectifying diode according to claim 1 of the patent in suit differs from the rectifier disclosed in document D2 essentially in that
 - (i) it is the second epitaxial layer, i.e. the layer not in contact with the substrate, which acts as the blocking layer under reverse bias condition (feature (f) of claim 1, see point V. above), and in that
 - (ii) the minimum thickness of the blocking layer is specified in dependence of the carrier concentration of this layer (feature (g)).
- 3.3.3 The rectifying diode described in the embodiment shown in Figure 3 of the patent in suit achieves a reverse breakdown voltage of about 400 V and has a reverse recovery time of about 10 ns (cf. column 11, lines 21 to 24 and 45 to 50; column 12, lines 8 to 11). The overall properties of this rectifying diode are, therefore, similar to the ones disclosed in document D2.

In consequence, having regard to document D2, the objective problem addressed by the patent in suit is to provide an alternative structure having at least the same performance as the rectifying diodes disclosed in this document.

3.3.4 A skilled person does not derive from document D2 that a rectifying diode with the blocking layer which is not in contact with the substrate would have overall properties as good as the ones of a diode in which the blocking layer is adjacent to the substrate. - 15 -

This view is further confirmed by document D11 which states that it is advantageous to start with a heavily doped n-type substrate and successively deposit a high resistivity (no intentional doping) epitaxial layer and a p-type epitaxial layer on it (cf. page 105, full last paragraph). Non-intentionally doped layers have, however, n-type conductivity, since nitrogen, a donor impurity, is practically always present (cf. the sentence bridging pages 106 and 107). In consequence, the structure suggested in this general background article as being advantageous for producing SiC rectifying diodes has the blocking layer in contact with the substrate, i.e. the same structure as the one employed by the authors of documents D1 and D2. In consequence, taking account of the common general knowledge in the art, there was no reason to expect that a rectifying diode in which the blocking layer is not provided directly in contact with the substrate would have acceptable overall properties. Furthermore, the overall properties of a SiC rectifying diode cannot be deduced from general theoretical considerations alone, but are a matter of practical experimentation based on these considerations.

4. For the foregoing reasons, in the Board's judgement, the subject-matter of claim 1 involves an inventive step in the sense of Article 56 EPC, having regard to the prior art and the general background knowledge of the skilled person.

> Dependent claims 2 to 18 concern further particular embodiments of the invention and are patentable for the same reasons.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

D. Spigarelli

R. K. Shukla