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D E C I S I O N
of 7 July 1999

Case Number: T 0581/97 - 3.5.2

Application Number: 89312504.7

Publication Number: 0371814

IPC: HO3K 17/78

Language of the proceedings: EN

Title of invention:
Light-sensitive semiconductor device

Patentee:
Sharp Kabushiki Kaisha

Opponent:
Siemens AG

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - no"

Decisions cited:
-

Catchword:
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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0581/97 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 7 July 1999

Appellant: (Proprietor of the patent)
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Representative:
-

Decision under appeal:
Decision of the Opposition Division of the European Patent Office posted 2 April 1997 revoking European patent No. 0 371 814 pursuant to Article 102(1) EPC.

Composition of the Board:

Chairman: A. G. Hagenbucher
Members: R. G. O'Connell
B. J. Schachenmann

Summary of Facts and Submissions

I. The appellant contests the decision of the opposition division to revoke European patent No. 371 814 on the ground that the subject-matter of the independent claims of the main and second auxiliary requests then on file did not involve an inventive step having regard to document

D2: US-A-4 777 387 and

common general knowledge in the art. The opposition division found that the first auxiliary request then on file contravened Article 123(3) EPC.

II. In a communication annexed to a summons to oral proceedings, the board referred to the following textbooks

D6: Tietze & Schenk: "Halbleiter-Schaltungstechnik", 7th edition, 1985, pages 83, 211 to 217 and

D7: McCarthy: "MOS Device and Circuit Design", 1982, pages 124 to 126, 132, 133

as substantiation of the assertion as to common general knowledge in the art relied on in the decision under appeal.

III. In reply thereto the appellant maintained only the claims corresponding to the second auxiliary request refused by the opposition division.

IV. During the oral proceedings, held on 7 July 1999, the

appellant filed the corresponding claims 1 to 5 as a single request.

V. Independent claim 1 is worded as follows:

"1. A semiconductor device comprising: a normally-off first MOSFET (1); a second transistor (2) connected between the gate and the source of the first MOSFET (1); a diode (3) connected between the gate and the source of the second transistor (2); and an optoelectric transducer array (4) connected between the gate and the drain of the second transistor (2);

the semiconductor device being characterised in that the second transistor (2) is a normally-off second MOSFET;

in that a resistor (5) is connected between the gate and the drain of the second transistor (2), the resistor (5) and the transducer array (4) being in parallel;

in that all the components of the semiconductor device are formed on a single semiconductor chip;

wherein said first and second MOSFETs are of the n-channel type"

Claims 2 to 5 depend on claim 1.

VI. The appellant argued essentially as follows:

The inventors of the opposed patent were originally confronted with three prior art light-sensitive semiconductor relays shown in Figures 5 to 7 of EP-A-371 814 (EP-B1-371 814, Figures 4 to 6). The Figure 5 (EP-A-371 814) circuit (without resistor 43) had the disadvantage that the output MOSFET ("normally-

off first MOSFET") took a long time to turn off following extinction of the light input to the photodiode array (optoelectric transducer array) because the release of the positive charge stored at the gate of the output MOSFET through the photodiode array took considerable time. The circuits shown in Figures 6 and 7 tried to decrease the turn-off time by means of a second MOSFET discharging the gate of the first MOSFET. According to Figure 6 of the patent application a normally off n-channel MOSFET was used for discharging. However, two photovoltaic arrays (optoelectric transducer arrays) and consequently too much space were necessary. The prior art shown in Figure 7 avoided the use of two photovoltaic arrays but had the disadvantage of mixed polarity MOSFETs. The invention as claimed and shown in Figure 1 avoided the disadvantages of these prior art solutions by using two n-channel MOSFETs and a single optoelectric transducer array. Document D2 showed in Figures 1 to 3 three prior art circuits. Figure 3 of D2 corresponded essentially to Figure 6 of the opposed patent with a p- and an n-channel MOSFET. Although document D7, which emphasised the attraction of the higher charge carrier mobility of n-channel devices and pointed to the poorer packing density and increased process complexity of the CMOS technique, was known before the filing date of D2, nevertheless D2 taught the use of MOSFETs with mixed polarity channels. D2 mainly tried to obviate the use of two optoelectric transducer arrays and showed only that this was possible with a CMOS technique. Figure 2 of EP-A-371 814 which was deleted during the examination procedure showed an alternative solution with two n-channel MOSFETs which was not within the scope of present claim 1 but also solved the problem

underlying the opposed patent. The respondent had not explained why in the light of this alternative a skilled person starting from D2 would have necessarily arrived at the claimed invention. It was not a case of a one-way street; there were at least two ways. Once an invention had been made it was always possible to explain how it could have been arrived at. But this was not the correct test. It was necessary to show, how a person skilled in the art having no knowledge of the present invention would have been motivated to arrive at the solution falling within the scope of claim 1. Document D2 showed the use of mixed polarity channels in connection with only one photovoltaic array, but did not hint at the claimed invention.

VII. The respondent argued essentially as follows:

The closest prior art relays with monolithic implementations were shown in D2 (Figures 1, 3, claim 6 and column 4, lines 9 to 11; column 5, lines 12 to 14). According to claim 6 of D2 the normally off transistor 21 of Figure 1 was replaced by a MOSFET. In Figure 3 of D2 the function of transistor 21 was implemented by a p-channel MOSFET whereas the output transistor was an n-channel MOSFET. The person skilled in the art knew that the use of MOSFETs with different polarity channels on the same semiconductor chip had disadvantages, namely poor packing density and increased process complexity; see D7, page 132, last paragraph. Starting from D2 (Figure 1) the problem arose how to implement the known monolithic relay in a simple and economical way. The person skilled in the art knew that the manufacture of monolithic circuits with n-MOSFETS only, ie one polarity, was easier than

with mixed polarity (see D6, page 216, second paragraph) and that for the output stage of the semiconductor device an n-MOSFET with its associated high charge-carrier mobility was necessary in view of the desired power. It was also known that when replacing p-channel MOSFETs by n-channel MOSFETs the polarities of the voltages, diodes and capacitors had to be inverted; see D6, page 83, penultimate paragraph. In view of the above problem the person skilled in the art would therefore have implemented the relays shown in Figures 1 and 3 of D2 by using only n-channel MOSFETs, with consequential inversion of the drive circuitry of the discharging MOSFET, including its resistor and diode, with respect to the gate, thus arriving directly at the claimed solution.

VIII. The appellant (proprietor) requested that the decision under appeal be set aside and that the patent be maintained in amended form with claims 1 to 5 as filed at the oral proceedings, description pages 1 and 12 as originally filed, pages 2 to 11, 13, 15 to 18 received 21 June 1993, page 5a received 7 June 1999, page 19 as amended with the response dated 14 July 1995; drawings according to EP-B1-371 814.

IX. The respondent (opponent) requested that the appeal be dismissed.

Reasons for the Decision

1. The appeal is admissible.

2. The main issue to be considered in the present appeal

is whether the subject-matter of claim 1 involves an inventive step having regard to D2 and common general knowledge in the art.

2.1 Closest prior art and problem to be solved.

In the prior art document D2 Figs 1 and 3 show alternative semiconductor circuit implementations of the same optical relay function. D2 explicitly suggests a partial monolithic implementation of the circuit of Figure 1 and a more complete monolithic implementation of the circuit of Figure 3. The latter has a normally-off first (output) MOSFET (17) and a normally-off second MOSFET (41) connected to the gate of the first MOSFET. A diode (14) is located between the gate and source of the second MOSFET. In Figure 3 the resistors 22 and 31 are connected between the gate and drain of the second MOSFET but according to the simpler version shown in Figure 1 a single resistor 22 is connected between the base and collector of the second transistor, the resistor and the transducer array being in parallel. A similar circuit is acknowledged as prior art in Figure 6 of the opposed patent. The latter refers to the disadvantage of this prior art circuit, namely that it involves the use of increased numbers of processes and masks for the manufacture of a semiconductor chip having both channel conductivity types; see column 3, lines 22 to 34 of EP-B1-371 814.

The problem underlying the opposed patent is therefore to provide a semiconductor device as specified in the preamble of claim 1 which can be fabricated on a single chip more easily with reduced numbers of process steps and masks and consequent saving of space.

2.2 According to claim 1 this is achieved by replacing the discharging p-channel MOSFET in D2 (Figure 3) or the transistor 21 in D2 (Figure 1) by an n-channel MOSFET, with a consequential relocation of the gate-source (base-emitter) diode and of the gate-drain (base-collector) resistor.

2.3 The known disadvantage, viz increased process complexity, of using MOSFETs with mixed polarity channels on a single semi-conductor chip, is already mentioned in column 3, lines 22 to 34 of the opposed patent. The prior art makes it clear that the first (output) MOSFET, being a power MOSFET, has to be implemented in n-channel technology in view of its better conductivity and smaller space requirement. It is common general knowledge in the art that NMOS technology avoids the disadvantage of mixed polarity channels and has the attraction of higher electron mobility compared to hole conduction; see D6, first paragraph of chapter 9.4.7 and D7, pages 124 to 126, 132 (last paragraph) and 133. It follows that a person skilled in the art who wishes to fabricate the semiconductor parts of D2 in a reduced number of process steps will try to implement the Figure 1 or 3 embodiments of D2 by using only n-MOSFETs. It is also notorious in this art (cf eg D6, in particular page 83) that replacing a MOSFET of one channel conductivity type by a MOSFET of the opposite channel conductivity type involves a consequential exchange of the polarities of the line voltages and pole reversal of diodes and electrolytic capacitors. Hence, the person skilled in the art will for the implementation of the components 14, 21 and 17 of Figure 1 in a pure MOSFET version (cf D2, column 4, lines 9 to 16, 41 to 42 and

claim 6) choose an n-MOSFET instead of transistor 21 and insert it in inverted position with respect to the MOSFET 41 of Figure 3. It follows from circuit function that the resistor 22 must be kept in the collector (or drain) - base (gate) branch and diode 14 in the emitter (or source) - base (gate) branch. Consequently the gate branches are inverted together with the MOSFET in view of the change of the channel polarity.

2.4 The appellant argued that although document D7 emphasising the advantages of n-channel devices was known before the priority date of document D2, nevertheless D2 showed only the use of mixed polarity channels and did not suggest anywhere that only n-channel MOSFETs should be used. It has to be borne in mind however that D2 is primarily concerned with the problem of obviating the use of several optoelectric transducer arrays while still achieving a rapid discharge of the gate of the power MOSFET (cf D2 column 1, lines 18 to 23, 54 to 64, 67 to column 2, line 13 and also Figure 5 of the opposed patent). Although, as has been referred to above, D2 explicitly refers to the possibilty of various degrees of integration in a monolithic implementation of the relay circuits described, in the judgement of the board, this reference is to be seen as largely aspirational at the priority date of D2 when power MOSFET circuitry was still dominated by discrete component technology. The detail of this integration, in particular optimising the fabrication process in terms of numbers of process steps and masks, was not a foreground consideration for the inventor of D2 - in contrast to the situation of the person skilled in the art addressing the problem underlying claim 1 of the opposed patent.

The appellant pointed also to Figure 2 as originally filed in the present patent application in order to show that several solutions using only n-channel MOSFETs were possible, but outside the scope of present claim 1 so that it was not a one way street; there were at least two ways. In contrast to the solutions in D2, the Figure 2 embodiment originally filed in the application which led to the opposed patent (but deleted during the examination procedure) concerns a solution with a normally-on n-channel second MOSFET whereas D2 teaches the use of a more economical and therefore preferable normally-off second MOSFET as claimed. Moreover, the solution shown in original Figure 2 would require a further resistor element. As the board understands the one-way street metaphor it implies that the person skilled in the art routinely avoids obviously disadvantageous side-turnings.

3. To sum up, the board concurs with the view of the opposition division that the semiconductor device specified in claim 1 results from routine efforts to optimise the fabrication of the semiconductor circuits known from D2. For these reasons, the board finds that the subject-matter of claim 1 does not involve an inventive step within the meaning of Article 56 EPC. Therefore the patent cannot be maintained.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Kiehl A. Hagenbucher