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D E C I S I O N
of 30 August 2001

Case Number: T 0736/97 - 3.4.3

Application Number: 91120395.8

Publication Number: 0488283

IPC: H01L 27/108

Language of the proceedings: EN

Title of invention:

Method of fabricating memory cell for semiconductor integrated circuit

Applicant:

NEC CORPORATOIN

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 56

Keyword:

"Inventive step: yes"

Decisions cited:

-

Catchword:

-



Case Number: T 0736/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 30 August 2001

Appellant:

NEC CORPORATION
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Minato-ku
Tokyo (JP)

Representative:

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Decision under appeal:

Decision of the Examining Division of the
European Patent Office posted 10 February 1997
refusing European patent application
No. 91 120 0395.8 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: R. K. Shukla
Members: M. Chomentowski
M. B. Günzel

Summary of Facts and Submissions

I. European patent application No. 91 120 395.8 (Publication No. 0488 283) was refused by the decision of the examining division dated 10 February 1997 on the ground that the subject-matter of the claims lacked an inventive step having regard to the prior art documents

D1: Japanese Journal of Applied Physics; Supplements (18th conference on Solid State Devices and Materials, Tokyo, 20th to 22nd August 1986), pages 257-260; K. Yamada: "Thermodynamical approach to a new high dielectric capacitor structure: W / HfO₂/ W",

D2: EP-A-0 338 157, and

D4: EP-A-0 175 433.

Claim 1 is the only independent claim of the set of claims forming the basis of the decision of the examining division and it reads as follows:

"1. A method of fabricating a capacitor of a memory cell which consists of a MOS transistor and a capacitor for a semiconductor integrated circuit, comprising the steps of:

a) forming a lower electrode (6, 7) having a predefined shape on a semiconductor layer (4, 5);

b) forming a first insulating interlayer (8) on entire surface of said semiconductor layer;

c) forming a photoresist (9) on entire surface of said first insulating interlayer (8);

d) etching said photoresist (9) and said first insulating interlayer (8) at a equal etching rate until the surface of said lower electrode (6, 7) is exposed to the same level as the insulating interlayer (8);

e) forming a strontium titanate dielectric (10) by radio-frequency sputtering method on said lower electrode (7) and on said insulating layer; and

f) forming an upper electrode (11) on said strontium titanate dielectric, said upper electrode constituting a capacitor with said lower electrode through said strontium titanate dielectric."

II. In the decision, the examining division reasoned essentially as follows:

The method of claim 1 differs from the method known from document D1 in that

- (i) it uses strontium titanate formed by rf-sputtering in place of hafnium oxide as the dielectric; and
- (ii) the photoresist and the first insulating interlayer are etched at an equal etching rate until the surface of the lower electrode is exposed at the same level as the insulating interlayer.

Strontium titanate as a dielectric film of a capacitor is known from document D2. The two dielectric materials strontium titanate and hafnium oxide are thus arbitrarily interchangeable. Moreover, it is clear that for an isolating dielectric material only rf-sputtering is applicable since dc-sputtering would result in the accumulation of positive charges.

Indeed, document D1 (see Figure 2) does not show a planarized a structure wherein the metal lines encounter no discontinuities or sharp edges. However, it is clear that the process according to Figure 2 of document D1 needs modifications if it is to be suitable for the formation of ultra-high density DRAMs mentioned on page 260, right-hand column, last five lines. In particular, a real life DRAM capacitor would never show protrusions over which a metal line has to be deposited; the capacitor which had to be investigated for research purposes did not of course have to satisfy these stringent conditions. These points are so obvious to the skilled engineer that they are hardly ever mentioned in publications. If one studies the available prior art, one can however deduce these requirements. In document D4 (see Figure 4), a DRAM structure is shown, albeit of a completely different type to that of the contested application, where the total available top surface of the silicon mesa is used as one capacitor electrode and the overlying metal line is flat. The use of a sacrificial layer for obtaining such a flat structure is therefore a process step of which the skilled person would immediately think for planarization.

Therefore, the subject-matter of claim 1 lacks an inventive step.

III. The applicant lodged an appeal against the decision on 10 April 1997, paying the appeal fee on the same day. A statement setting out the grounds of the appeal was filed on 27 May 1997.

IV. In the communication issued on 2 May 2001, the Board informed the appellant that claim 1, the only independent claim of the set of 2 claims submitted with the statement setting out the grounds of the appeal, appeared to lack clarity and indicated amendments to

claim 1 which could meet the objections. Further, amendments to page 4 of the description were indicated for consistency with the proposed wording of the claim.

- V. With the letter of 1 August 2001, the appellant expressed his agreement with the proposed amendments.
- VI. The appellant requests that the decision under appeal be set aside and that a patent be granted on the basis of the following patent application documents:

Description:

pages 1, 2 and 5, as filed;
pages 2a, 3, 6 and 10, filed during the oral proceedings of 9 January 1997 before the examining division;
page 4 attached to the communication of the Board issued on 2 May 2001 and approved by the appellant in his letter dated 1 August 2001;

Claims:

Nos. 1 and 2 attached to the communication of the Board issued on 2 May 2001 and approved by the appellant in his letter dated 1 August 2001;

Drawings:

Sheet 1/3, as filed.

As compared to claim 1 forming the basis of the decision under appeal, present claim 1 additionally specifies, in particular, that only the entire top surface of the lower electrode is exposed during the etch-back step of the method, and it reads as follows:

"1. A method of fabricating a capacitor of a memory cell which consists of a MOS transistor and a capacitor for a semiconductor integrated circuit, comprising the steps of:

a) forming a lower electrode (6, 7) having a predefined shape on a semiconductor layer (4, 5);

b) forming a first insulating interlayer (8) on the entire surface of said semiconductor layer, the first insulating interlayer covering the lower electrode;

c) forming a photoresist (9) on the entire surface of said first insulating interlayer (8);

d) etching said photoresist (9) and said first insulating interlayer (8) at an equal etching rate so as to expose only the entire top surface of said lower electrode (6, 7) at the same level as the insulating interlayer (8);

e) forming a strontium titanate dielectric (10) by radio-frequency sputtering method on said exposed top surface of the lower electrode (7) and on said insulating layer; and

f) forming an upper electrode (11) on said strontium titanate dielectric, said upper electrode constituting a capacitor with said lower electrode through said strontium titanate dielectric."

(emphasis added by the Board)

VII. The appellant submitted the following arguments in support of his request:

Starting from document D1, an object of the present invention is to provide a method of fabricating a memory cell for a semiconductor integrated circuit, which can realize a higher degree of integration, and to prevent a reduction in yield due to disconnections in wiring formed after the formation of a capacitor.

This object is achieved by

- (i) using strontium titanate formed by rf-sputtering in place of hafnium oxide as the dielectric; and
- (ii) etching the photoresist and the first insulating interlayer at an equal etching rate to expose only the top surface of said lower electrode at the same level as the insulating interlayer.

Concerning the distinguishing feature (i), there is no indication in any of documents D2, wherein strontium titanate is mentioned, and D1 that these two dielectric materials are arbitrarily interchangeable. The radio-frequency sputtering deposition method of strontium titanate is not disclosed in document D2 and leads to a dielectric film with decreased thickness. It is argued in the decision under appeal that it is clear that for an isolating dielectric material only rf-sputtering is applicable since dc-sputtering would result in the accumulation of positive charges. However, since this process feature is not disclosed in document D2, it cannot be considered as obvious.

Feature (ii) leads to a further improvement of the memory cell since it allows to reduce the memory cell area by employing the entire upper surface of the lower electrode. Moreover, the leakage current between the

upper and lower electrodes of the capacitor can be prevented by utilizing a flat structure without decreasing the film thickness of the dielectric film at the end of the lower electrode.

Document D1 (see Figure 2) does not show a planarized structure wherein the metal lines encounter no discontinuities or sharp edges. Figure 5 of

D3: Patent Abstracts of Japan, vol. 12, No. 254
(E-634) (3101), 16 July 1988 & JP-A-63-042164

also shows an upper electrode (7) which has not been planarized. Concerning document D4, which as admitted in the decision under appeal corresponds to a completely different DRAM structure, it shows a flat overlaying metal film extending over the total available top surface of a silicon mesa capacitor electrode; however, there are structural features, for instance in Figure 6, with the sides surface of the mesa being also used as a capacitor electrode, and method features, for instance the oxidation of the silicon mesa for forming the dielectric, which are totally different from those of the present invention. In this respect, it is argued in the decision under appeal that it is clear that the process according to Figure 2 of document D1 needs modifications if it is to be suitable for the formation of ultra-high density DRAMs. However, document D1 gives no indication as to which kind of modifications a person skilled in the art will have to perform.

It is also to be noted that the argument in the decision under appeal that planarization processes are so obvious to skilled engineers that they are hardly ever mentioned in publications cannot be accepted,

because, if a feature is not mentioned in the state of the art, the assumption must be that this feature is not obvious.

Therefore, the subject-matter of claim 1 involves an inventive step.

Reasons for the Decision

1. The appeal is admissible.
2. *Article 123(2) EPC and Article 84 EPC*

Amendments to claim 1 in relation to claim 1 as originally filed are highlighted in the wording of claim 1 in item V above. The amendments are based on the embodiment of the invention described with reference to Figures 1A to 1E on page 4, line 26 to page 6, line 21.

The description and the Figures have been amended for consistency with claim 1 and they relate only to the embodiment of Figures 1A to 1E.

The Board is therefore satisfied that the application as amended complies with Article 123(2) EPC.

Moreover, in view of the amendments to the description and the Figures, there is no inconsistency between the present claims and the application as amended.

Therefore, the Board is satisfied that the present claims are supported by the description in the sense of Article 84 EPC.

3. The only issue in the present case is that of inventive step.

3.1 A method of fabricating a capacitor of a memory cell which consists of a MOS transistor and a capacitor for a semiconductor integrated circuit is known from document D1 (see in particular Figure 2 and the corresponding text; see also page 260, right-hand column, last five lines). From the whole content of the document, it is derivable that the method comprises the steps of:

- (a) forming a lower electrode of tungsten having a predefined shape on a semiconductor layer;
- (b) forming a first insulating interlayer (SiO_2) on the entire surface of said semiconductor layer, the first insulating interlayer covering the lower electrode;
- (c) forming a photoresist on the entire surface of said first insulating interlayer (SiO_2);
- (d) etching said photoresist and said first insulating interlayer (8) so as to expose the top surface of said lower electrode (W);
- (e) forming a dielectric (HfO_2) on said exposed top surface of the lower electrode (W) and on said insulating layer (SiO_2); and
- (f) forming an upper electrode (W) on said dielectric, said upper electrode constituting a capacitor with said lower electrode through said dielectric.

The method of present claim 1 differs from this known method in that,

- (i) in steps (e) and (f), it uses strontium titanate formed by rf-sputtering in place of hafnium oxide as the dielectric; and
- (ii) in step (d) the photoresist and the first insulating interlayer are etched at an equal etching rate to expose only the entire top surface of said lower electrode at the same level as the insulating interlayer.

3.2 Starting from document D1, an object of the present invention is to provide a method of fabricating a memory cell for a semiconductor integrated circuit, which can realize a higher degree of integration, and to prevent a reduction in yield due to disconnections in wiring formed after the formation of a capacitor.

This object is credibly achieved by the method of claim 1.

3.3 With regard to the distinguishing feature (ii), the Board agrees with the appellant that this allows to reduce the memory cell area by employing the entire upper surface of the lower electrode. Moreover, the leakage current between the upper and lower electrodes of the capacitor can be prevented by utilizing a flat structure without decreasing the film thickness of the dielectric film at the end of the lower electrode.

Document D1 (see Figure 2) on the other hand does not show a planarized structure and the metal lines have discontinuities or sharp edges. Figure 5 of D3 also shows an upper electrode (7) which has not been planarized. Document D4 shows a flat overlaying metal film extending over the total available top surface of

a silicon mesa capacitor electrode. However, there are structural features, for instance in Figure 6, with the side surfaces of the mesa being also used as a capacitor electrode, and method features, for instance the oxidation of the silicon mesa for forming the dielectric, which are totally different from those of the present invention. Thus document D4 is not concerned with a planarized capacitive structure, and does not disclose an etching step as set out in distinguishing feature (ii).

- 3.4 Document D2 (see in particular column 7, lines 5 to 14 and 33 to 35) concerns DRAM cells wherein the capacitor is formed with a PZT (lead zirconium titanate) dielectric by sputtering or evaporation; strontium titanate being mentioned as an alternative to PZT.

It is argued in the decision under appeal that

- the skilled person would have recognized that the structure of Figure 2 of document D2 must be planarized, and
- that planarization processes are so obvious to skilled engineers that they are hardly ever mentioned in publications.

In absence of any evidence showing that the structure of Figure 2 of document D2 entailed a planarization process as claimed, the Board is not persuaded by the mere assertion in the decision under appeal that the distinguishing feature (ii) was rendered obvious by the disclosure in document D2.

3.5 With regard to feature (i), the Board is not convinced by the arguments of the examining division that hafnium oxide and strontium titanate are arbitrarily exchangeable. This is because, in document D2, the dielectric material strontium titanate is used for its ferroelectric properties, whereas in document D1 the dielectric materials are not required to be ferroelectric.

3.6 For the foregoing reasons, in the Board's judgment, the subject-matter of claim 1 is not obvious having regard to the state of the art and it thus involves an inventive step in the sense of Article 56 EPC.

Consequently, claim 1 is patentable in the sense of Article 52(1) EPC.

Claim 2 is a dependent claim and is patentable for the same reasons.

4. Consequently, oral proceedings requested auxiliarily by the appellant are not necessary.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the examining division with the order to grant a patent on the basis of the following patent application documents:

Description:

pages 1, 2 and 5, as filed;
pages 2a, 3, 6 and 10, filed during the oral proceedings of 9 January 1997 before the examining division;
page 4 attached to the communication of the Board issued on 2 May 2001 and agreed to by the appellant with the letter of 1 August 2001;

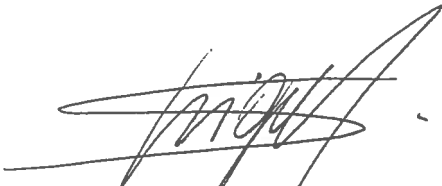
Claims:

Nos. 1 and 2 attached to the communication of the Board issued on 2 May 2001 and agreed to by the appellant with the letter of 1 August 2001;

Drawings:


Sheet 1/3, as filed.

The Registrar:



D. Spigarelli

The Chairman:



R. K. Shukla

Order

the above reasons as we believe that

the above order is not in the

best interests of the community and the

order is hereby rescinded and the

order is hereby rescinded.

Respectfully,

James L. [Name]

Mayor of the City of [City]

City of [City], [State]

Signature

Date: [Date]

Printed Name: [Name]

Title: [Title]

City of [City], [State]

City of [City], [State]

City of [City], [State]

Signature

Date: [Date]

City of [City]

City of [City]

City of [City]

City of [City]

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