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**D E C I S I O N**  
**of 2 March 2001**

**Case Number:** T 0859/97 - 3.4.3

**Application Number:** 92830542.4

**Publication Number:** 0591599

**IPC:** H01L 21/336

**Language of the proceedings:** EN

**Title of invention:**

Method of fabricating integrated devices, and integrated device produced thereby

**Applicant:**

STMicroelectronics S.r.l.

**Opponent:**

-

**Headword:**

Inverse T-Gate/STM

**Relevant legal provisions:**

EPC Art. 56, 84  
EPC R. 67

**Keyword:**

"Inventive step (yes) - after amendments"  
"Refund of the appeal fee (no)"  
"Essential features - present in the claim"

**Decisions cited:**

T 1055/92

**Catchword:**

-





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Boards of Appeal

Chambres de recours

**Case Number:** T 0859/97 - 3.4.3

**D E C I S I O N**  
**of the Technical Board of Appeal 3.4.3**  
**of 2 March 2001**

**Appellant:** STMicroelectronics S.r.l.  
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**Representative:** Cerbaro, Elena, Dr.  
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**Decision under appeal:** Decision of the Examining Division of the  
European Patent Office posted 18 April 1997  
refusing European patent application  
No. 92 830 542.4 pursuant to Article 97(1) EPC.

**Composition of the Board:**

**Chairman:** R. K. Shukla  
**Members:** G. L. Eliasson  
A. C. G. Lindqvist

## Summary of Facts and Submissions

- I. European patent application No. 92 830 542.4 was refused in a decision of the examining division dated 18 April 1997. The ground for the refusal was that the subject matter of independent claim 7 as originally filed was not new with respect to either of the prior art documents
- D1: International Electron Devices Meeting, Technical Digest, December 1989, pages 765 to 768; and
- D2: IEEE Electron Device Letters, vol. 11, May 1990, pages 221 to 223.
- II. The reasoning of the examining division in the decision under appeal can be summarized as follows:
- (a) Document D1 discloses a MOS device having a layered gate structure comprising a first polycrystalline silicon gate region, an oxide layer, and a second polycrystalline silicon gate region on the oxide layer. The two polysilicon gate regions are electrically connected via a polysilicon sidewall layer. Although Figure 1 of document D1 only shows a cross-section of the gate structure along a first direction across the source and drain regions, it necessarily follows from the manufacturing steps described in document D1 that the polysilicon sidewall layer extends along all sides of the gate. Thus, the polysilicon sidewall layer forms an electric contact also at the end portions of the gate in the direction perpendicular to the plane of Figure 1. Therefore,

the subject matter of claim 7 is not new. The same reasoning also applies *mutatis mutandis* in respect of document D2 disclosing a similar device to that disclosed in document D1.

(b) Although not forming part of the reasons for the refusal, the examining division referred to the objections under Article 84 EPC raised against method claims 1 to 6 in the official communication dated 22 November 1995. In particular, the following features considered to be essential were lacking in claim 1: (i) ion-implantation for forming source/drain regions (26, 29, 37, 38); (ii) spacers 33 for forming the self-aligned structure; and (iii) a gate oxide layer 11.

II. The appellant (applicant) lodged an appeal on 4 June 1997, paying the appeal fee on 28 May 1997. A statement of grounds of the appeal was filed on 4 August 1997 together with new claims.

III. In response to a communication of the Board, the appellant filed with the letter dated 13 December 2000 new claims 1 to 9.

The appellant requests that the decision under appeal be set aside and that a patent be granted based on the following documents:

**Claims:** 1 to 9 filed with the letter dated  
13 December 2000

**Description:** Pages 1 to 12 as filed

**Drawings:** Sheets 1/3 to 3/3 as filed

The appellant furthermore requests reimbursement of the appeal fee, and oral proceedings in case the Board intended to dismiss the appeal.

IV. Independent claims 1 and 7 read as follows:

"1. A method of fabricating integrated devices in a substrate (2) of semiconductor material, said method comprising steps of:  
depositing a first polycrystalline silicon layer (12) over said substrate; depositing a layer of insulating material (13) on said first polycrystalline silicon layer; depositing at least a second polycrystalline silicon layer (17) over said layer of insulating material; selectively etching said second polycrystalline silicon layer for forming first gate regions (18) of a first length in a first direction; forming, in said substrate, first substrate regions (26, 29) in alignment with said first gate regions, extending laterally therefrom and having a first doping level; selectively etching said first polycrystalline silicon layer for forming second gate regions (12) of a second length, greater than said first length, in said first direction; and forming, in said substrate, second substrate regions (37, 38) in alignment with said second gate regions and partially overlapping said first substrate regions, said second substrate regions having a second doping level greater than said first doping level;  
characterized by the fact that said step of depositing a second polycrystalline silicon layer (17) is preceded by the step of shaping said layer of insulating material (13) for forming insulating

portions of insulating material, having a predetermined width in a second direction perpendicular to said first direction; and by the fact that, during said step of depositing said second polycrystalline silicon layer (17), a portion of said second polycrystalline silicon layer extends laterally beyond said insulating portions in said second direction, so that said portion of said second polycrystalline silicon layer electrically contacts said first polycrystalline silicon layer (12)."

- "7. An integrated device in a substrate (2) of semiconductor material, comprising a first polycrystalline silicon gate region (12) of a first length in a first direction; an insulating material region (13) on said first gate region; a second polycrystalline silicon gate region (18) over said insulating material region and of a second length, less than said first length, in said first direction; first substrate regions (37, 38) embedded in said substrate in alignment with the first gate region (12), extending laterally therefrom and having a first doping level; and second substrate regions (26,29) embedded in said substrate in alignment with the second gate region (18) and extending laterally therefrom beneath said first gate region (12) and partially overlapping said first substrate regions (37, 38), said second substrate regions presenting a second doping level lower than said first doping level; said insulating material region (13) having a predetermined width in a second direction perpendicular to said first direction; the device

further comprising field oxide regions (1) surrounding said device at least in said second direction, wherein a portion of said second gate region (18) extends over said field oxide regions and laterally beyond said insulating material region (13) in said second direction, whereby said portion of said second gate region (18) is in direct electrical contact with said first gate region (12)."

Claims 2 to 6, 8 and 9 are dependent claims.

V. The appellant presented essentially the following arguments in support of his requests:

(a) The device and method of producing the device, as claimed, both specify that the first and second gate regions are in direct contact with each other in a region extending from the insulating region in the second direction. This construction provides an improved contact over that of the device of document D1 where a thin polysilicon sidewall layer is used which is prone to oxidation resulting in a poor contact.

(b) The appellant requests reimbursement of the appeals fee, for the following reason:

(i) The appellant had informed the examining division that the statements relating to the deposition of the polysilicon on "short sidewalls" in the official communication pursuant to Article 96(2) EPC, were not understood by the applicant. The refusal of the application after a first communication



thus deprived the applicant of an opportunity to overcome a novelty objection which was not clear.

(ii) Moreover, the appellant contends that the statements in point 3 of the decision under appeal, to the effect that etching of the thick polysilicon layer 18 and the oxide layer 13 down to the lower polysilicon layer 12, as illustrated in the second drawing from the top of Figure 1 in document D1, would also result in the "same lateral dimension" (first and second directions) of the these two layers, constitutes a fresh argument presented for the first time in the decision under appeal, so that the appellant has had no opportunity to respond to this argument.

(iii) Finally, since the refusal was concerned only with claims 7 to 10 as filed and did not discuss the patentability of claims 1 to 6, the applicant was not given the possibility to cancel the rejected claims and request further examination on the other claims.

### **Reasons for the Decision**

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.
2. *Amendments and clarity*

2.1 Claim 1 contains the features of claim 1 as filed and has been amended for clarity. Independent claim 7 corresponds to claims 7 and 8 as filed and contains clarifying amendments. Claims 2 to 6 and 8 to 9 correspond to claims 2 to 6 and 9 to 10 as filed.

The Board is therefore satisfied that the claims as amended meet the requirements of Article 123(2) EPC.

2.2 Regarding claims 1 to 6, the decision under appeal referred to the objection raised in the official communication dated 22 November 1995 where it was held that claim 1 was not clear since it did not include all the essential features of the invention (cf. item II(b) above). The appellant has in the statement of the grounds of appeal merely referred to the arguments given in his letter dated 28 March 1996 where a reference to the case T 1055/92 (OJ EPO, 1995, 214) was made. In this connection, as was held in T 1055/92, point 5, features which are described as essential in the application for solving the technical problem addressed by the invention must be present in an independent claim in order that the claim is supported by the description as required by Article 84 EPC, second sentence.

In the present case, the invention as disclosed is concerned with improving electrical connection between first and second gate portions, which are mutually isolated by an intervening insulating layer, of an inverted T-shaped gate electrode. In the invention as described, this is achieved by extending the polysilicon layers of the first and second gate portions in a second direction (as defined in the claim), beyond the insulating layer. It is evident from

the description that neither the presence of a gate oxide, the spacers on the sidewalls of the second gate region, nor the use of ion-implantation to form source/drain regions is essential for achieving the stated object of the invention. Thus, the features listed in item II(b) above are not essential to the invention. Also, in the Board's view, the invention as defined by the claim is consistent with the invention as disclosed, and the claim is thus supported by the description, as required by Article 84 EPC, second sentence.

Furthermore, claim 1 now makes it clear that the first and second substrate regions (source/drain regions) are formed in alignment with the first and second gate regions, respectively, so that the role of the first and second gate regions for defining the extent of the first and second substrate regions is clear.

In the Board's opinion, therefore, the claims are clear and contain all essential features, thereby meeting the requirements of Article 84 EPC.

3. *Novelty - claim 1*

3.1 The application in suit relates to MOSFETs having double diffused source and drain regions and a so-called "Inverse T" gate structure: The lower portion of the gate is wider in a first direction and defines the limits for the highly doped portions of the source/drain regions, whereas the short upper portion of the gate defines the distance between the portions of the source/drain regions having a low doping level. In order to realize such a structure, it is necessary to form an etch stop layer of e.g. a thin oxide layer

between the two portions of the gate electrode. A thin oxide layer, however, has the disadvantage of electrically isolating the upper and lower gate portions from each other.

The present invention solves this problem by contacting the upper and lower polysilicon layers in a portion which is extending in a second direction, perpendicular to the first direction, outside the active device region.

- 3.2 Document D1 discloses a method of producing a MOSFET having an inverse-T gate structure (cf. Figure 1). The method includes the steps of forming a first polysilicon layer over a substrate, then an oxide layer on the first polysilicon layer and subsequently a second polysilicon layer on the oxide layer. After patterning and etching the second polysilicon layer to form the first gate region, the exposed oxide layer is removed, and ion-implantation is carried out to form lightly doped regions. A polysilicon sidewall layer is deposited on the sidewall of the first gate region and on the first polysilicon layer, whereby the polysilicon sidewall layer provides electrical connection between the first and second gate regions. The first polysilicon layer is then etched to form the second gate region having a length greater than the length of the first gate region in a first direction.

A similar method is disclosed in document D2 as well, where a polysilicon sidewall layer is used for providing an electrical connection between the first and second gate regions (cf. Figure 1).

- 3.3 The method of claim 1 differs from that of document D1

(and from that of document D2) in particular in that (a) the insulating material on the first polycrystalline silicon layer is shaped to have a predetermined width in a second direction perpendicular to the first direction; and (b) subsequently the second polysilicon layer is deposited on the patterned insulating material and on the first polysilicon layer so that a portion of the second polysilicon layer extending beyond the patterned insulating material is directly in electrical contact with the first polysilicon layer.

In the method disclosed in document D1 (or in document D2), on the other hand, the insulating layer is not patterned prior to the deposition of the second polysilicon layer, so that the latter is not in direct contact with the first polysilicon layer. A further polysilicon layer on the sidewalls of the first gate region is required to provide the electrical contact between the first and second gate regions.

The subject matter of claim 1 is thus new with respect to the cited prior art documents D1 and D2.

4. *Inventive step - claim 1*

4.1 In the decision under appeal, the examining division did not raise any objections against novelty or inventive step of the subject matter of claim 1. The Board is also of the view that the subject matter of claim 1 is not rendered obvious by the cited prior art for the following reasons:

4.1.1 The claimed method has the advantage over the known method in that the contact area between the first and

second gate regions can be made larger in the second direction, thereby enabling a more reliable connection with a low contact resistance. Furthermore, the claimed method requires one less step of depositing polysilicon on the sidewall than the method of either document D1 or document D2.

- 4.1.2 In the Board's opinion, a skilled person faced with the above technical problem of improving the method of either document D1 or document D2 would not be able to arrive at the method of claim 1 in an obvious matter, since the available prior art does not contain any suggestion to modify the known method.

Therefore, the subject matter of claim 1 involves an inventive step as defined in Article 56 EPC.

5. *Novelty - claim 7*

- 5.1 It follows from the discussion of document D1 in points 3.2 and 3.3 above that the method of document D1 leads to a device having a gate structure different from the gate structure of the device as set out in claim 7. The device of independent claim 7 specifies that the upper, second gate region is shorter than the lower, first gate region in the first direction (source-drain direction), and that in the second direction, a portion of the first gate region extends beyond the active device region and is in direct contact with the second gate region. The device of document D1, on the other hand, has a polysilicon sidewall layer establishing an electric contact between the upper and lower polysilicon layers.

- 5.2 In the decision under appeal, the examining division

identified the first gate region with the lower polysilicon layer and the second gate region with the upper polysilicon layer and the polysilicon sidewall layer, and argued that since the first and second gate regions in the device of document D1 must have end portions in the second direction which lie outside the active device region, the device of document D1 must also have a contact region in the second direction outside the active device region.

Although the Board fully agrees with the above assessment of the disclosure of document D1 by the examining division, claim 7 as amended specifies that the first and second gate regions have different lengths in the first direction, in contrast to the corresponding gate regions in the device of document D1 which have the same length in the first direction.

- 5.3 The same argument applies *mutatis mutandis* when comparing the device of claim 7 with that of document D2.

Thus, the subject matter of claim 7 is new with respect to document D1 or D2.

6. *Inventive step - claim 7*

As discussed under point 4 above for claim 1, the Board does not see any hint in the prior art which would lead the skilled person to modify the device of document D1, or that of document D2, in such a manner to arrive at the device of claim 7. Therefore, the subject matter of claim 7 involve an inventive step (Article 56 EPC).

7. For the reasons above, claims 1 and 7 meet the

requirements of Article 52(1) EPC.

Dependent claims 2 to 6, 8, and 9 also therefore comply with the requirements of Article 52(1) EPC.

8. *Reimbursement of the appeal fee*

8.1 The appellant has requested a refund of the appeal fee for the reasons stated under points V(b)(i) to (iii) above. Under Rule 67 EPC, the appeal fee can only be reimbursed when the appeal is allowable, and a reimbursement is equitable by reason of a substantial procedural violation. It is therefore necessary to investigate whether the examining division committed a substantial procedural violation or not.

8.1.1 Regarding the appellant's submission that he did not understand the objection raised by the examining division (cf. item V(b)(i) above), the Board has compared the content of the official communication dated 22 November 1995 with that of the decision under appeal, and finds that the reasons for the finding of lack of novelty leading to the refusal of the application in item 2 of the decision under appeal are exactly the same as those communicated to the applicant in the above-mentioned communication (cf. point 3.1). Moreover, in the Board's view, for a person skilled in the integrated circuit device technology, the discussion of the prior art document in point 3.1 of the communication was clear and comprehensible, so that the applicant was given the opportunity to present his comments on the finding of lack of novelty.

It is also noted that the appellant did not avail himself of the opportunity to request oral proceedings



in his response of 28 March 1996. Such a precautionary request for oral proceedings provides an opportunity to clarify any outstanding issue and safeguards against any adverse decision by the examining division which should be considered a likely outcome when, as in the present case, the applicant's response did not contain any amendments to the claims to meet the objection raised by the examining division.

8.1.2 As to the submission of the appellant that point 3 of the decision under appeal contains arguments put forward for the first time (cf. point V(b)(ii) above), the Board notes that although these arguments are presented for the first time in the decision under appeal, they do not form the basis for the finding of lack of novelty: Moreover, they do not introduce any new fact or evidence, but merely explain the already cited passages of document D1 in more detail.

8.1.3 Regarding the argument that the decision under appeal only concerned a part of the claims (cf. point V(b)(iii) above), it is sufficient for the examining division, when deciding to refuse a European patent application under Article 97(1) EPC, to state one ground only which in their opinion would prejudice the grant of a European patent, since the EPC does not contain any provision which would allow a European patent to be partially granted. In the present case, the examining division was unable to grant a patent because it was of the opinion that the subject matter of claim 7 was not new. Consequently, the examining division was under no obligation to comment on the patentability of claims 1 to 6.

8.2 Thus, for the foregoing reasons, in the Board's

judgement, the examining division did not commit a procedural violation in issuing the decision to refuse the application. Therefore, the requirements of Rule 67 EPC for allowing a reimbursement of the appeal fee are not met. The appellant's request for the refund of the appeal fee is therefore not well-founded and is accordingly rejected.

## **Order**

### **For these reasons it is decided that:**

1. The decision under appeal is set aside.
2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the documents as specified under item III above.
3. The request for refund of the appeals fee is rejected.

The Registrar:

The Chairman:

L. Martinuzzi

R. K. Shukla