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D E C I S I O N
of 8 July 2002

Case Number: T 1033/97 - 3.4.3

Application Number: 91107384.9

Publication Number: 0463330

IPC: H01L 21/90

Language of the proceedings: EN

Title of invention:
Iterative self-aligned contact metallization process

Applicant:
TEXAS INSTRUMENTS INCORPORATED

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

Case Number: T 1033/97 - 3.4.3

D E C I S I O N
of the Technical Board of Appeal 3.4.3
of 8 July 2002

Appellant: TEXAS INSTRUMENTS INCORPORATED
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 6 May 1997 refusing European patent application No. 91 107 384.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. K. Shukla
Members: V. L. P. Frank
M. B. Günzel

Summary of Facts and Submissions

I. The appeal lies against the decision of the Examining Division dated 6 May 1997 refusing the European patent application No. 91 107 384.9. The ground for the refusal was that the subject-matter of claim 1 according to both the main and auxiliary requests did not involve an inventive step (Article 56 EPC), having regard to the following prior art document:

D2: EP-A-0 010 596

II. The appellant (applicant) lodged an appeal on 14 July 1997, paying the appeal fee the same day. The statement setting out the grounds of appeal together with claims 1 to 6 of the auxiliary request forming the basis of the decision were filed on 16 September 1997.

III. In response to a communication from the Board, the appellant filed on 14 June 2002 a revised page 4 of the description and a revised claim 1.

The wording of the only independent claim 1 is as follows:

"1. A method of forming multiple layers of interconnections in an integrated circuit, comprising the steps of:

forming a first conductor layer (28, 50);

forming a first insulator (24, 52) on said first conductor layer (28, 50);

forming a second conductor layer (50, 62) on said

first insulator layer (24, 52);

forming a second insulator layer (52, 64) on said second conductor layer (50, 62);

forming first (56, 66) and second (54, 68) cavities each having a first depth and having sidewalls extending through said second insulator layer (52, 64) and said second conductor layer (50, 62), said first cavity (56, 66) being wider than said second cavity (54, 68);

conformally depositing a third insulator layer (58, 70) on said second insulator layer (52, 64) such that sidewall insulators (60, 72) are deposited on said sidewalls of said first cavity (56, 66) and such that said second cavity (54, 68) is substantially filled with said insulator;

anisotropically etching through said first cavity (56, 66) to a second depth to expose a portion of said first conductor layer (28, 50) while retaining the sidewall insulators (60, 72); and

conformally depositing a third conductor layer (62, 74) on said third insulator layer (58, 70) such that said third conductor layer (62, 74) extends through said first cavity (56, 66) to contact said first conductor layer (28, 50)."

IV. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the following patent application documents:

Claims: 1 filed on 14 June 2002 with the letter

dated 14 June 2002
2 to 6 filed on 16 September 1997 with the letter dated 16 September 1997

Description: pages 3 and 5 to 12 as originally filed
page 1 filed on 10 April 1995 with the letter dated 7 April 1995
pages 2, 2a filed on 2 February 1996 with the letter dated 1 February 1996
page 4 filed on 14 June 2002 with the letter dated 14 June 2002

Drawings: Sheets 1/3 to 3/3 filed on 28 August 1991 with the letter dated 26 August 1991

V. In the decision under appeal the Examining Division argued essentially as follows:

Document D2 represents the closest state of the art. The method defined by claim 1 of the auxiliary request differs from the method disclosed in this document in that the layer formed on the first conductor layer is an insulator one and in that the wider cavity is etched to a second depth to expose the first conductor layer (cf. D2, Figure 6 and the corresponding text). The first difference does not, however, involve an inventive step, since a skilled person would apply the method known from document D2 to a different layer stack with the same technical aim of contacting a buried conductive layer (ie an "analogous use" situation, cf. Guidelines C-IV, 9.8, A1, v). Furthermore, the step of etching through the wider cavity to expose the lower conductor is a direct consequence of applying the method of document D2 to

this different layer stack in order to expose the first conductor layer.

VI. The appellant argued essentially as follows in support of his request:

There exist several important differences between the prior art disclosed in document D2 and the method according to the application:

(a) Document D2 discloses a different layer order than the one specified in claim 1 of the application.

(b) In the document the two cavities are formed separately from each other in two successive etching steps. As a result, one cavity is deeper than the other (cf. D2, page 15, lines 5 to 6). In contrast, the present invention requires that both cavities be formed in the same step and have the same depth.

(c) According to the application in suit, the wider cavity is etched to a second depth and through the insulating layer overlying the lowest conductor. According to the method of document D2 the second layer of the stack order (ie the second conductor layer) has already been removed from the wider cavity during the step of forming the cavities.

Moreover, the problem addressed by the application in suit is to find a simple method of interconnecting several conductor layers of an integrated circuit. This is a completely different problem than the one stated in document D2, ie the reduction of dimensions of surface areas of semiconductor arrangements, and a

skilled person would not be encouraged by the teaching of this document to modify the method disclosed therein.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

In the decision under appeal, there were no objections against claim 1 of the auxiliary request under Article 123(2) EPC, and the Board is also satisfied that the claim as amended during the examination proceedings complied with Article 123(2) EPC.

During the appeal proceedings the penultimate paragraph of claim 1 was amended in relation to claim 1 of the auxiliary request forming the basis of the decision as highlighted below:

"**anisotropically** etching through said first cavity (56, 66) to a second depth to expose a portion of said first conductor layer (28, 50) **while retaining the sidewall insulators (60, 72)**; and"

These amendments clarify the type of etch process performed. They are based on the disclosure at column 6, lines 18 to 21, lines 29 to 33 and Figure 2d of the published application.

The description was further amended to reflect the amendments made to the independent claim.

The Board is, therefore, satisfied that these amendments fulfill the requirement of Article 123(2) EPC.

3. *Inventive step*

The only issue in this appeal is that of inventive step.

3.1 Large scale integrated circuits require interconnections of a large number of functional devices in a single semiconductor chip. To this end, a three-dimensional structure of interconnecting planes is used. It is, however, necessary that the successively formed insulator and conductor layers have a planar surface so that further interconnection layers can be formed thereon. Furthermore, "vertical" interconnections are required between conducting layers formed on different planes while avoiding at the same time electrical contact with intermediate conductive layers.

The application in suit discloses a method for contacting a buried interconnection layer while avoiding contact to other intermediate conductive layers, and for simultaneously forming interelement isolation regions. The method can be employed iteratively, as it enables to produce a planar surface on which further processing can be carried out.

3.2 It is not disputed by the appellant that document D2 is the closest state of the art. The technical problem addressed by this document is to enable the achievement of submicron resolution by using conventional lithographic techniques (cf. page 3, lines 33 to

page 4, line 5). The method comprises the conformal deposition of an insulating layer 18 on a substrate 10 having several cavities formed in it. A reactive ion etch anisotropically removes the "horizontal" parts of the insulating layer 18, leaving an insulating layer on the sidewalls in the cavities. The presence of the insulating layer on the sidewalls reduces the lateral size of the cavities by the thickness of the remaining insulating layer, allowing to achieve submicron resolution at the bottom of the cavities (cf. Figures 1A to 1C and page 6, lines 1 to page 7, line 25). It is stated that the method can be applied on different kind of substrates usually used for manufacturing semiconductor devices (cf. page 4, lines 21 to 27).

3.3 Document D2 further discloses a method for contacting a buried conducting region, while avoiding contacting other intermediate conducting layers, and for providing a wall-like interelement isolation structure between adjacent regions (cf. page 14, line 4 to page 15, line 28; Figures 6A to 6D). According to this embodiment, a multilayer structure consisting of a n^+-type layer 63, a n^--type layer 64 and an insulator layer 65 is formed in this order on a p^--type substrate 60. Wide and narrow cavities extending up to the substrate, ie the layer to be electrically contacted, are then formed. An insulator layer 80 is then conformally deposited on this structure so that the narrow cavities are completely filled by the insulator 80 and form wall-like interelement isolation structures whereas in the wide cavities the insulator layer covers the sidewalls and the horizontal bottom walls. The "horizontal" regions of the insulator layer 80 are then removed by a reactive ion etching. This step leaves an

insulator layer on the sidewalls of the wide cavities. These cavities are filled with a conductor material 82 to provide an electric contact to the substrate.

Consequently, in this embodiment the following layer stack is used (cf. Figure 6D):

5. conductor layer 82 (top layer)
4. insulator layer 65
3. semiconductor layer 64
2. semiconductor layer 63
1. semiconductor layer 60 (bottom layer or substrate).

Moreover, the wide cavity for providing electrical contact is etched to extend to the layer to be contacted.

3.4 The method specified in claim 1 differs from the above prior art method in that

(i) the first layer 24 overlying the first (bottom) conductor layer 28 is an insulator layer instead of a semiconductor layer 63 as disclosed in document D2;

(ii) the wide and narrow cavities have a depth extending through the second insulator layer and the second conductor layer whereby the first insulating layer 24 overlying the first conductive layer onto which electrical contact is to be made is exposed; and in that

(iii) an etching step is carried out through the first (wider) cavity after the conformal deposition of the insulator layer 58 which fills the narrow

cavity, to expose a portion of the first conductor layer 28.

3.5 The effect achieved by these measures is that the cavities, and in particular the narrow cavity, are required to be initially opened to traverse only the two upper layers, ie the second insulator layer 52 and the second conductor layer 50, and do not need to traverse three layers as it is the case in the method disclosed in document D2. Since in the claimed method the layer overlying the bottom layer is an insulator layer, the second conductor layer 50 overlying this insulator layer is separated into isolated regions by the insulator in the narrow cavity. The narrow cavity can, therefore, be less deep than that in the state of the art. This is advantageous, since the filling of narrow cavities having a high aspect ratio is a difficult task.

The problem addressed by the application in suit can, therefore, be regarded as to improve the method disclosed in document D2.

3.6 The Examining Division argued in the decision under appeal that it would have been obvious for a skilled person to apply the method disclosed in document D2 to a stack having the layer sequence specified in the application in suit. In particular, it referred to the passage of document D2 stating that the disclosed method can be applied on many different kinds of substrates which are usually used for manufacturing semiconductor devices (cf. page 4, lines 21 to 27).

The Board, however, cannot concur with this reasoning, since the application of the prior art method to the

specified stack of layers would require that the first and second cavities are etched down to the layer to be electrically contacted, ie the first conductor layer 28, with the result that the narrow cavity would be deeper and more difficult to be filled by the conformally deposited insulator layer 52. The application of the method according to the embodiment of Figures 6A to 6D of document D2 to a stack of multiple conductor layers with intermediate insulating layers would not result in the provision of wide and narrow cavities extending up to the first insulating layer 24 as in the claimed method.

Moreover, the passage of document D2 cited by the Examining Division refers to the first embodiment, ie the achievement of submicron resolution using conventional lithographic techniques and not to the method described under point 3.3 above which is more relevant to the application in suit (cf. page 3, lines 33 to page 4, line 5).

3.7 The Board therefore comes to the conclusion that the method of forming multiple layers of interconnections in an integrated circuit using the layer sequence specified in claim 1 is not rendered obvious by the disclosure of document D2.

The two other documents considered during the examination procedure, ie Patent Abstracts of Japan, vol. 14, no. 421 (E-976), 11 September 1990 & JP-A-2 161 755 and Patent Abstracts of Japan, vol. 13, no. 338 (E-795) 28 July 1989 & JP-A-1 099 254, do not disclose the layer sequence specified in the application in suit. Moreover, both documents disclose to form cavities extending up to the layer to be electrically

contacted.

3.8 For these reasons, in the Board's judgement, the subject-matter of claim 1 involves an inventive step within the meaning of Article 56 EPC and accordingly meets the requirements of Article 52(1) EPC.

The dependent claims 2 to 6 concern further particular embodiments of the invention which are patentable for the same reasons.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the following documents:

Claims: 1 filed on 14 June 2002 with the letter dated 14 June 2002
2 to 6 filed on 16 September 1997 with the letter dated 16 September 1997

Description: pages 3 and 5 to 12 as originally filed
page 1 filed on 10 April 1995 with the letter dated 7 April 1995
pages 2 and 2a filed on 2 February 1996 with the letter dated 1 February 1996
page 4 filed on 14 June 2002 with the letter dated 14 June 2002

Drawings: sheets 1/3 to 3/3 filed on 28 August 1991 with the letter dated 26 August 1991

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla